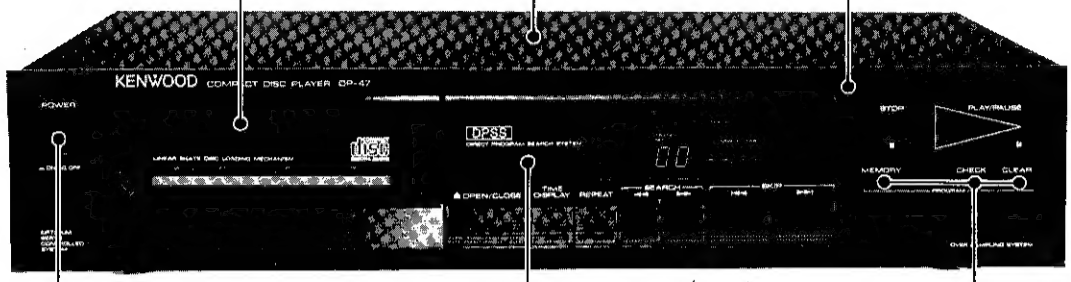
COMPACT DISC PLAYER

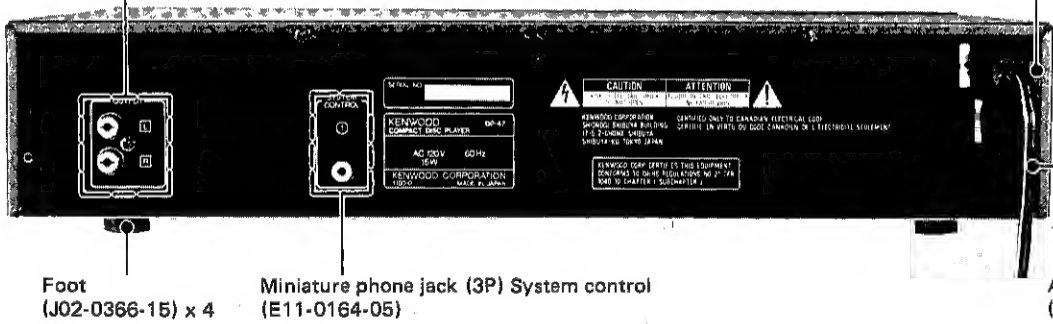
DP-47

SERVICE MANUAL

KENWOOD

B51-3446-00(O)2846





In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

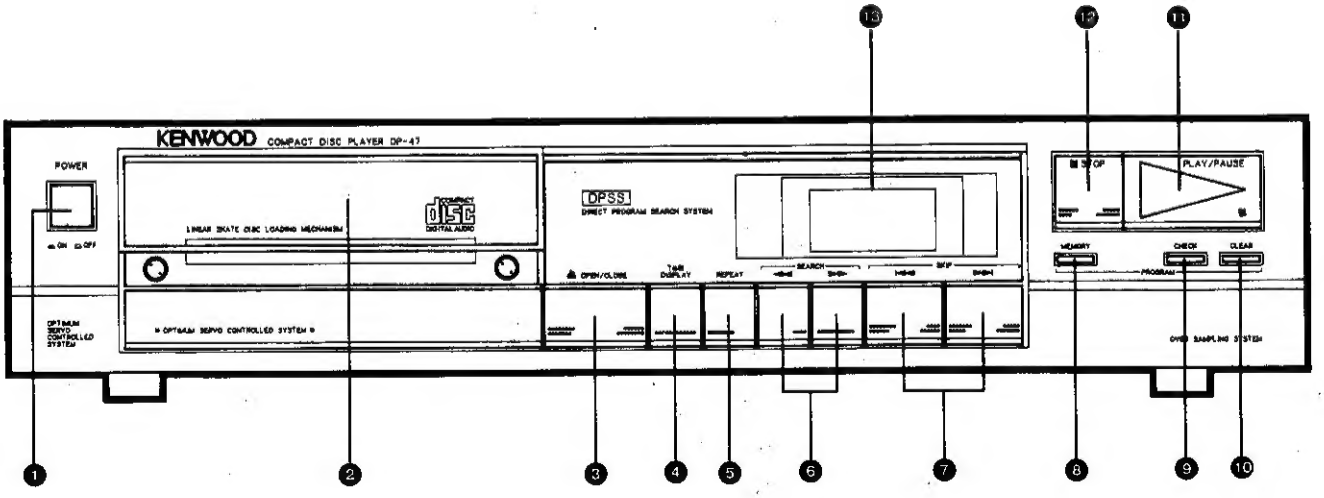
KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated. AVOID DIRECT EXPOSURE TO BEAM.

CONTENTS/CONTROLS AND INDICATORS

CONTROLS AND INDICATORS

Numbers in circles correspond to the diagram, symbols in brackets correspond to front panel indications.



CONTROL AND INDICATORS

❶ POWER switch
Press to turn the power ON.
Pressing again turns the power OFF.

❺ Disc tray
This will be opened or closed by pressing the OPEN/CLOSE (▲) key.
Place a disc on this tray with its label surface up.

❸ OPEN/CLOSE key (▲)
Used to open/close the disc tray.
When this key is pressed during play, the disc rotation will stop and the disc tray will be opened.
- When this key is pressed with the tray closed, the tray is opened.
  When it is pressed in the middle of tray opening, the tray will be closed.
- After the tray is closed, the disc information (TOC = Table Of Contents) will be read out and then the unit will enter the stop mode automatically.

❹ TIME display key
Used to select the desired time display.

❺ REPEAT key
Press this key to play the disc repeatedly.
The repeat function will be cancelled by pressing the REPEAT key again.

❻ SEARCH keys (◀◀, ▶▶)
Press to go quickly in the forward or backward direction.

❼ SKIP keys (|◀◀, ▶▶|)
Press to play the next track or the track being played from the beginning.

❽ MEMORY key
Used to store the desired track for programed play.
In the stop mode, select the desired tunes using the SKIP (|◀◀, ▶▶|) keys and then press the MEMORY key. The PGM indicator lights to show that the program track is stored in memory.

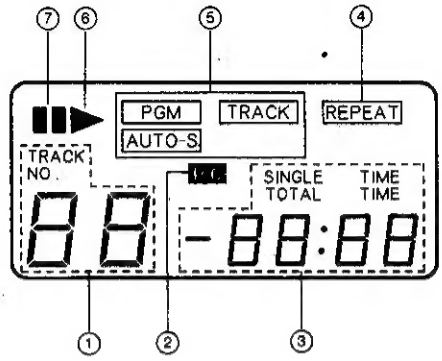
❾ CHECK key
Used to check the programmed contents.
The TIME display key is invalid during program checking.

❿ CLEAR key
Used to clear the programmed contents.

⓫ PLAY/PAUSE key (▷, ❚❚)
When this key is pressed, the play indicator lights (▶) and the play starts. When it is pressed again, the pause indicator (❚❚) lights and the unit enters the pause mode.
When the key is pressed with the tray opened, the tray is closed and then the play starts after the disc information (TOC) is read out. If the tracks are programmed using the MEMORY key, the memory play will be started.

⓬ STOP key (■)
When this key is pressed during play, the play stops.

⓭ Display window



① **Track number display (TRACK NO.)**

② **Program check indicator (P.C.)**
Lights when checking the programmed contents.

③ **Time counter display**
(SINGLE TIME/TOTAL TIME)
Displays the elapsed time of the tune or the total playing time of the disc or other time information.
For details, refer to page 13.
When inputting or checking the program, the program number is displayed.

④ **REPEAT indicator (REPEAT)**

⑤ **Play mode indicator**
Track mode indicator (TRACK)
This indicator lights when the play mode is set to normal play mode.

Program mode indicator (PGM)
This indicator lights when the play mode is set to programed play mode.

Auto space indicator (AUTO-S.)
This indicator lights when the auto-space function (providing a non-recorded blank of about 4 seconds between tunes) is activated. Auto Space function is available in Program mode.

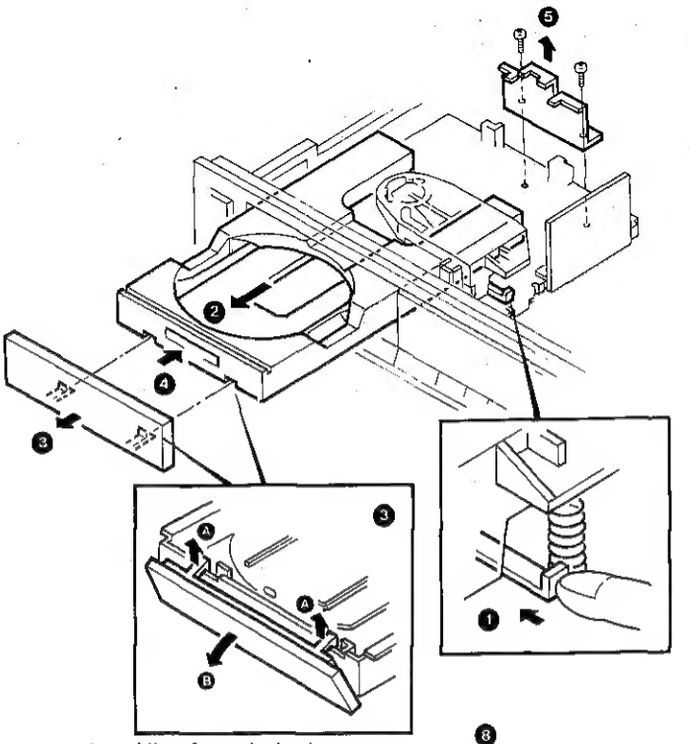
⑥ **Play indicator (▶)**
Lights in the play mode.

⑦ **Pause indicator (❚❚)**
Lights in the pause mode.

DISASSEMBLY FOR REPAIR

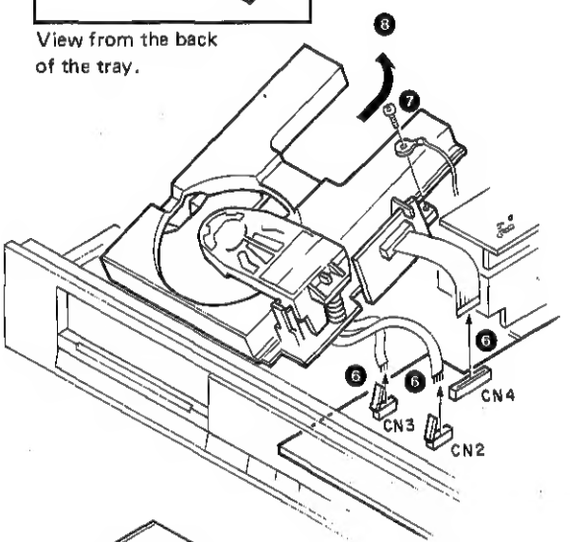
1. Removing the Mechanism Ass'y

1. Push the projection of the Slider Ass'y under the disc clamper in the direction of the arrow (❶). This will release the Slider Ass'y roller from the stop position.
2. Pull out the tray in the direction of the arrow (❷) gently by hand.
3. Disengage the 2 claws on the tray panel by pulling the panel lightly in the direction of the arrow (Ⓐ), and then remove the tray panel gently in the direction of arrow (Ⓑ) (❸).
4. Push the tray again in the direction of the arrow (❹).
5. Take out the metal hardware behind the mechanism by removing the 2 screws (❺).



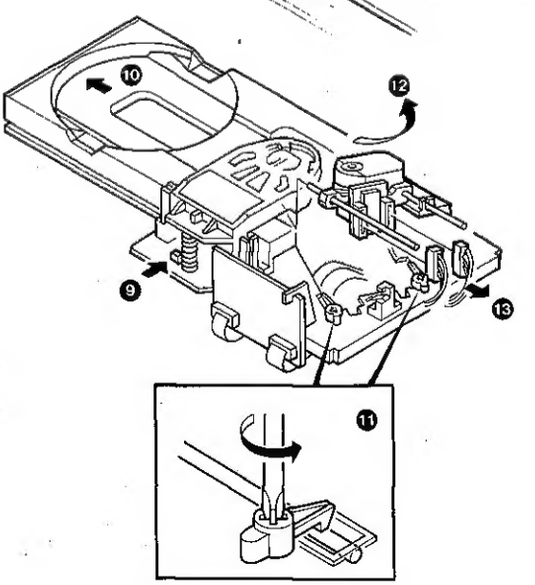
View from the back of the tray.

6. Remove the wires and flexible cable from the 3 connectors (CN2 CN3 and CN4) on the Main Unit (❻), and remove the grounding lug holding screw (❼).
7. Remove the Mechanism Ass'y in the direction of the arrow (❽).

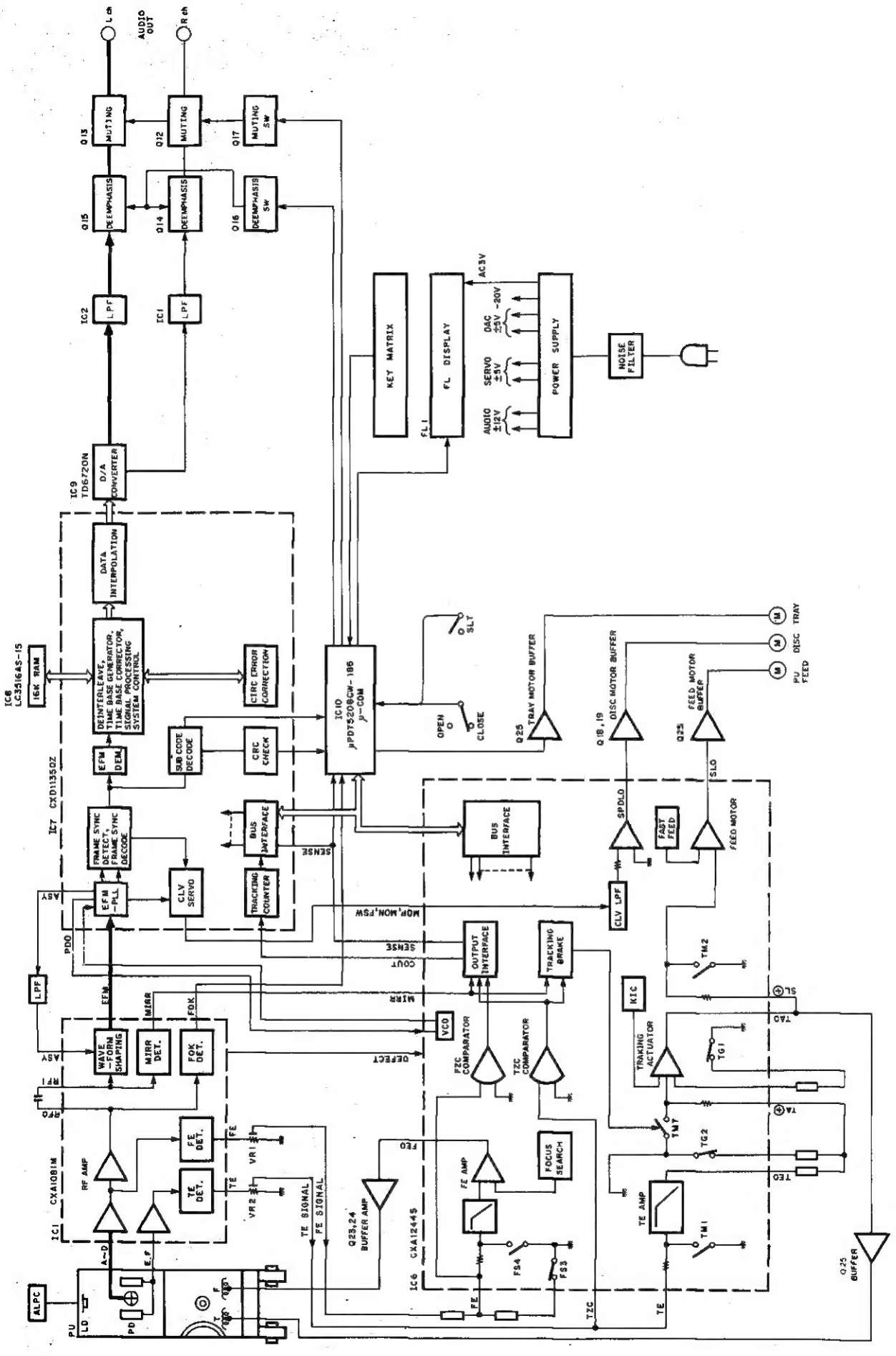


2. Removing the pickup

1. Push the projection on the Slider Ass'y under the disc clamper in the direction of the arrow (❾) again. Then pull out the tray in the direction of the arrow (❿).
2. Loosen the 2 pickup rail holding points using a screwdriver (⓫), and then take out the pickup in the direction of the arrow (⓬).
3. Disconnect the wires from the 2 pickup connectors (⓭).



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Description of components

1–1. ELECTRIC UNIT (X25-331X-XX)

Component		Use/Function	Operation/Condition/Compatibility
Ref. No.	Parts No.		
IC1, 2	M5218P or NJM4560D	Low pass filter	Eliminates sampling pulse.
IC4	M5218P	Op-amp.	(1/2) : Reset circuit. When the +5V power supply drops to +4.3V or below, the output goes "H", turning Q27 ON, which applies the power-off reset. (2/2) : Tray open/close circuit. The output is −5.5V when open, and +5.5V when closed.
IC5	M5218P	Op-amp.	(1/2) : PLL compensation circuit. (2/2) : CLV compensation circuit.
IC6	CXA1244S	Servo IC	Generates pulses for the focusing servo, tracking servo and feed servo.
IC7	CXD1135QZ	Digital signal processor LSI	Handles demodulation, correction and interpolation of EFM data, PLL circuit. Processes all digital signals, including the CLV servo signal.
IC8	LC3516AS-15	Static RAM	Signal processor RAM (16K).
IC9	TD6720N	D/A converter	Converts digital data into an analog quantity.
IC10	μPD75208CW-186	Microprocessor	Handles the display, key input processing and servo IC control.
IC11	M5218P	Op-amp.	Amplification of the error in the regulated analog ±5V power supply.
Q1	2SD1266(P,Q)	Ripple filter	Digital +5.3V ripple filter.
Q2	2SC945(A)(Q,P) or 2SC1740S(Q,R)	Ripple filter	Digital +5.3V ripple filter.
Q3, 4	2SA954(L,K)	Ripple filter	Digital −5.1V ripple filter.
Q5	2SC2003(L,K)	Ripple filter	Analog +6.1V ripple filter.
Q6	2SA954(L,K)	Ripple filter	Analog −6.1V ripple filter.
Q7, 8	2SA954(L,K)	Ripple filter	Analog +5V ripple filter.
Q9	2SC2003(L,K)	Ripple filter	Analog −5V ripple filter.
Q10	2SA954(L,K)	Ripple filter	FL −31V ripple filter.
Q11	2SA733(A)(Q,P) or 2SA933(Q,R)	Ripple filter	FL −31V ripple filter.
Q12, 13	2SC2878(B)	Muting SW	LINE OUT muting switch.
Q14, 15	2SC2878(B)	De-emphasis SW	De-emphasis switch.
Q16	DTA124EN	Digital SW	De-emphasis switch.
Q17	2SC945(A)(Q,P) or 2SC1740S(Q,R)	SW	LINE OUT muting switch.
Q18	2SD822(Q,P)	Driver	Disc motor driver.
Q19	2SA1534A	Driver	Disc motor driver.
Q20	2SC945(A)(Q,P) or 2SC1740S(Q,R)	Buffer amp.	Amplifies the clock signal (16.9MHz).
Q21, 22	2SK246(Y,GR)	FET	Select switch for the TE and FE signals.
Q23	2SD1266(P,Q)	Driver	Focusing coil driver.
Q24	2SA1534A	Driver	Focusing coil driver.
Q25	STA341M	Driver	Tray open/close, tracking coil and sled motor driver.
Q26	2SA733(A)(Q,P) or 2SA933(Q,R)	SW	Turned ON by the signal at pin 21 (DEFECT) of CXA1081M.
Q27	2SC945(A) (Q,P) or 2SC1740S(Q,R)	SW	Discharges the power-on reset capacitor, C134.
Q28	2SD1266(P,Q)	Ripple filter	Digital +5.3V ripple filter.
Q29	2SC945(A)(Q,P) or 2SC1740S(Q,R)	SW	FE bias select switch.
Q31	2SC945(A)(Q,P) or 2SC1740S(Q,R)	Amp.	Amplifier for the anti-shock comparator.

1–2. CONTROL CIRCUIT UNIT (X29-1890-00)

Component		Use/Function	Operation/Condition/Compatibility
Ref. No.	Parts No.		
IC1	CXA1081M	RF amp.	Generation of focusing error signal and tracking error signal. Generation and phase compensation of RF signal. Auto-symmetry correction circuit.
Q1	2SA1426	SW	Laser diode power supply switch.
Q2	2SC945(A) (Q,P)	SW	FE bias select switch.

CIRCUIT DESCRIPTION

2. Set mode flow chart
(Simplified flowchart after power ON)

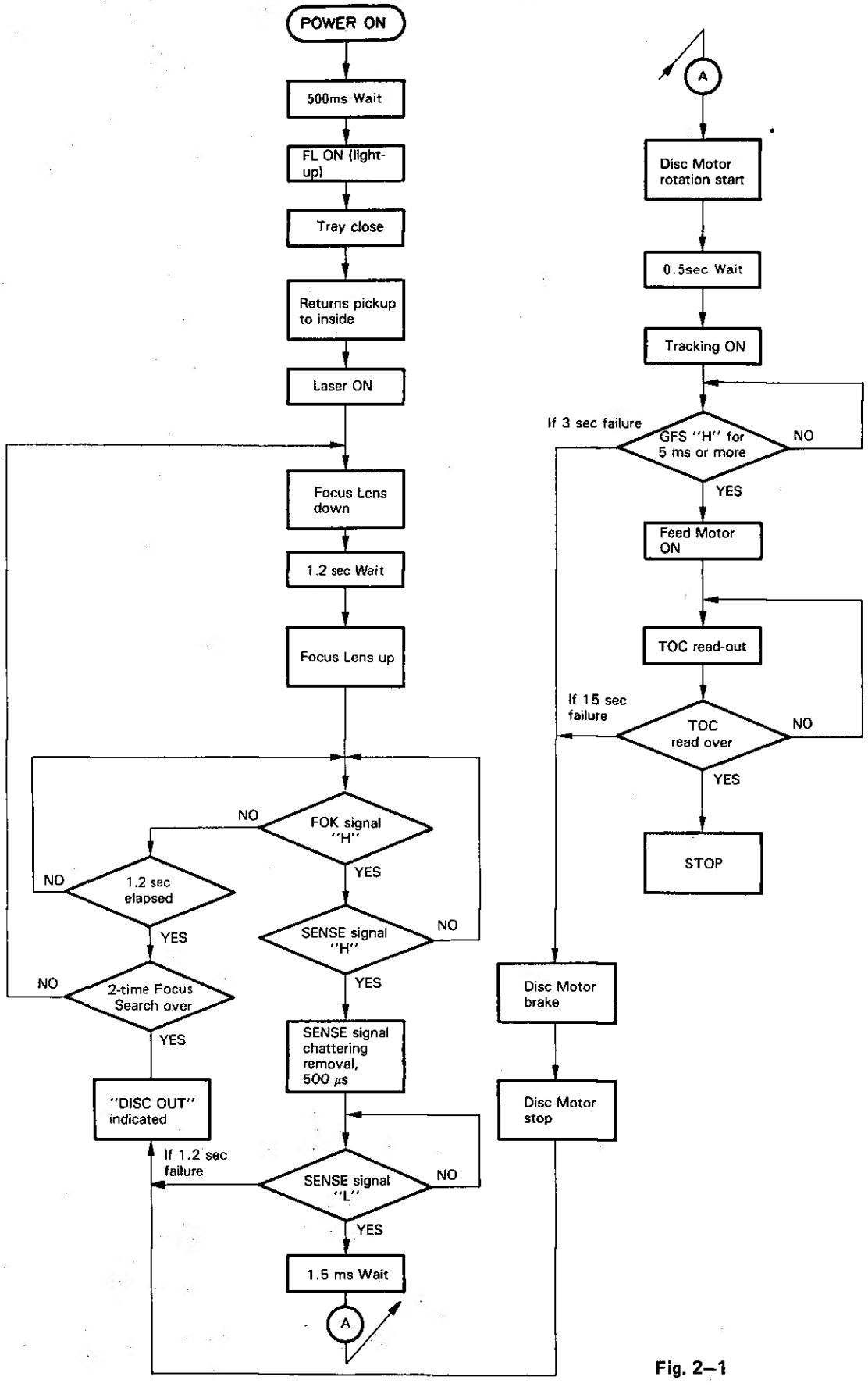


Fig. 2–1

CIRCUIT DESCRIPTION

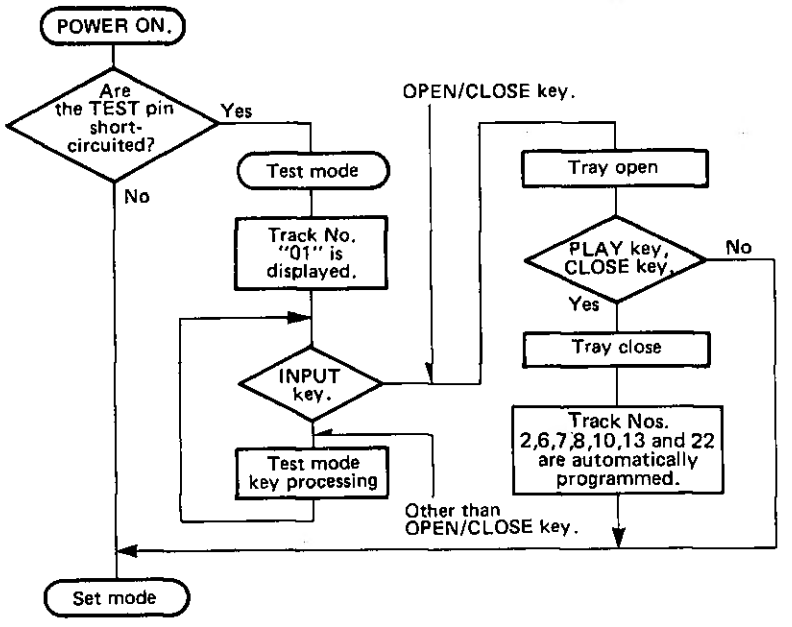
3. Test mode

If the TEST pins are short-circuited when the power is turned ON, the microprocessor enters test mode. With the microprocessor set to test mode, each operation can be easily checked after making a repaire or adjustment.

With the DP-47, the microprocessor can be set to test mode by short-circuiting pin 5 and pin 6 of the ELECTRIC UNIT (X25-331X-XX).

Note : "Set mode" shows the normal status.

3–1. Flow chart



3–2. Effective keys in the Test mode and their functions

No.	Input key	Function	Track No. dispaly
1	PLAY	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . ON. (3) Feed servo . . . . . ON. When the key is pressed in the Stop mode, the servoes are switched ON automatically in the order from (1) to (3).	TRACK NO. 05 ↓ Display for a few seconds after (1) to (3). ↓ Disc's Track No. is displayed.
2	CHECK	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . OFF. (3) Feed servo . . . . . OFF.	TRACK NO. 03
3	CLEAR	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . ON. (3) Feed servo . . . . . OFF.	TRACK NO. 04
4	STOP	(1) Focus servo . . . . . OFF. (2) Tracking servo . . . . . OFF. (3) Feed servo . . . . . OFF.	TRACK NO. 01
5	▶▶	In Stop mode : Moves the pickup slightly to the outer tracks. With feed servo ON : Switches the tracking gain to "H".	
6	◀◀	In Stop mode : Moves the pickup slightly to the inner tracks. With feed servo ON : Switches the tracking gain to "L".	
7	OPEN/CLOSE	When the tray is opened and the closed again in test mode, TRACK NOs 2, 6, 7, 8, 10, 13 and 22 are automatically programmed. Opening the tray again will cause the unit to enter set mode.	
8	MEMORY	FL is all light on.	

Table 3–1

CIRCUIT DESCRIPTION

4. Microprocesser μPD75208CW-186 (X25-331X-XX : IC10)

4–1. Terminal connection diagram

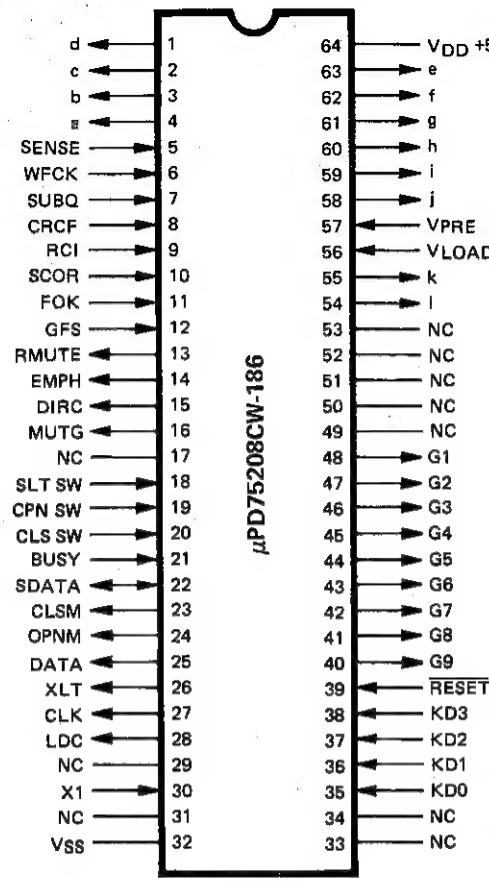


Fig. 4–1

4–2. Block diagram

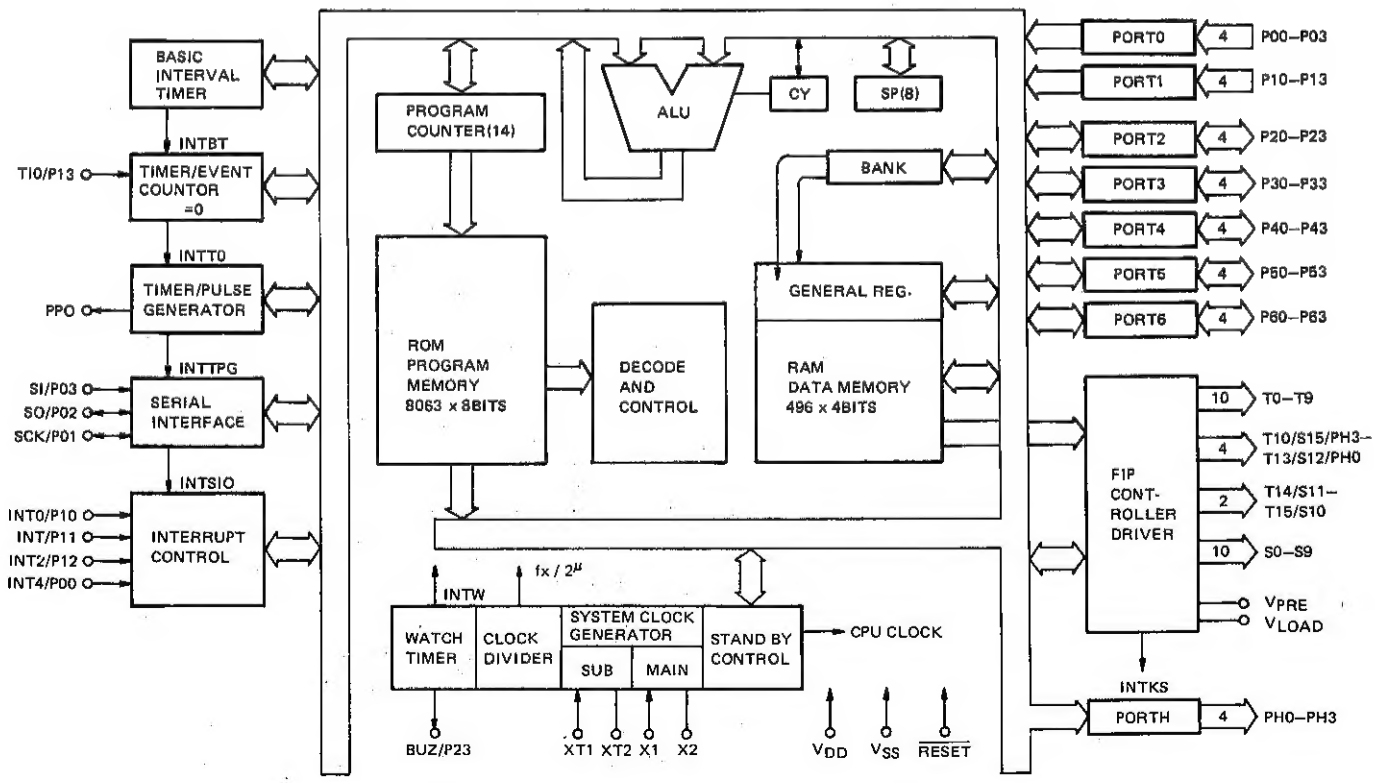


Fig. 4–2

CIRCUIT DESCRIPTION

4–3. Explanation of terminals

Terminal No.	Symbol	I/O	Terminal name	Function
1 ~ 4	S3 ~ S0	O	d ~ a	Control terminal of fluorescent indicator-tube segment. (Key scan signal)
5	P00/INT4	I	SENSE	Terminal for detecting SENSE outputs from signal processing IC (CXD1135QZ) and servo IC (CXA1244S).
6	P01/$\overline{SCK}$	I	WFCK	Input terminal of Q data reading clock (from CXD1135QZ).
7	P02/SO	I	SUBQ	Q data input terminal (from CXD1135QZ).
8	P03/SI	I	CRCF	Q data CRC inspection result input terminal. When CRCF : 1, OK. (from CXD1135QZ)
9	P10/INT0	I	RCI	Remote control signal input.
10	P11/INT1	I	SCOR	Sub code frame sync detection signal input terminal.
11	P12/INT2	I	FOK	FOK signal input terminal of RF amplifier (CXA1244S). When FOK : 1, there is reflected light.
12	P13/T10	I	GFS	Frame sync condition signal input terminal (from CXD1135QZ). When GFS : 1, frame sync is kept. When GFS : 0, frame sync is out.
13	P20	O	RMUTE	Analog mute control terminal. Active "L".
14	P21	O	EMPH	De-emphasis control terminal. Active "H".
15	P22	O	DIRC	Output terminal of DIRC terminal control signal of servo IC (to CXA1244S).
16	P23	O	MUTG	Output terminal of MUTG terminal control signal of signal processing IC (to CXD1135QZ).
17	P30	–	–	NC.
18	P31	I	SLT SW	Sled switch (limit switch) input terminal. When sled (Pickup) is at most inside, this is set to "L".
19	P32	I	OPN SW	Tray open switch input terminal. When tray is open, this is set to "L".
20	P33	I	CLS SW	Tray close switch input terminal. When tray is closed, this is set to "L".
21	P60	I	BUSY	Serial BUSY signal input terminal.
22	P61	I/O	SDATA	Serial data input/output terminal.
23	P62	O	CLSM	Tray motor CLOSE signal output terminal.
24	P63	O	OPNM	Tray motor OPEN signal output terminal.
25	P40	O	DATA	Data terminal control signal output terminal (to CXA1244S and CXD1135QZ).
26	P41	O	XLT	Latch terminal control signal output terminal (to CXA1244S and CXD1135QZ).
27	P42	O	CLK	Clock terminal control signal output terminal (to CXA1244S and CXD1135QZ).
28	P43	O	LDC	Laser ON/OFF signal output terminal. When ON,this is set to"H",and when OFF to"L".
29	PP0	–	–	NC.
30, 31	X1, X2	I/O	X1, X2	System clock input terminal.
32	Vss	–	Vss	GND.
33, 34	XT1, XT2	–	–	NC.
35 ~ 38	P50 ~ P53	I	KD0 ~ KD3	Key return signal input terminal of key matrix.
39	$\overline{RESET}$	I	RESET	Reset input terminal. Active "L".
40 ~ 48	T0 ~ T8	O	G9 ~ G1 (GRID)	Fluorescent indicator-tube digit control terminal.
49 ~ 53	T9 ~ T13	O	–	NC.
54, 55	S11, S10	O	l, k	Fluorescent indicator-tube segment control terminal.
56	V_{LOAD}	I	V_{LOAD}	Negative power supply for driving fluorescent indicator-tube (–30V).
57	V_{PRE}	I	V_{PRE}	Negative power supply for predriving fluorescent indicator-tube.
58 ~ 63	S9 ~ S4	O	j ~ e	Fluorescent indicator-tube segment control terminal (S4, S5 : Key scan signal).
64	V_{DD}	I	V_{DD}	Power supply terminal (+5V).

Table 4–1

CIRCUIT DESCRIPTION

5. RF AMP CXA1081M (X29-1890-00 : IC1)

General

The CXA1081M is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply.
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability.

Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

5–1. Block diagram

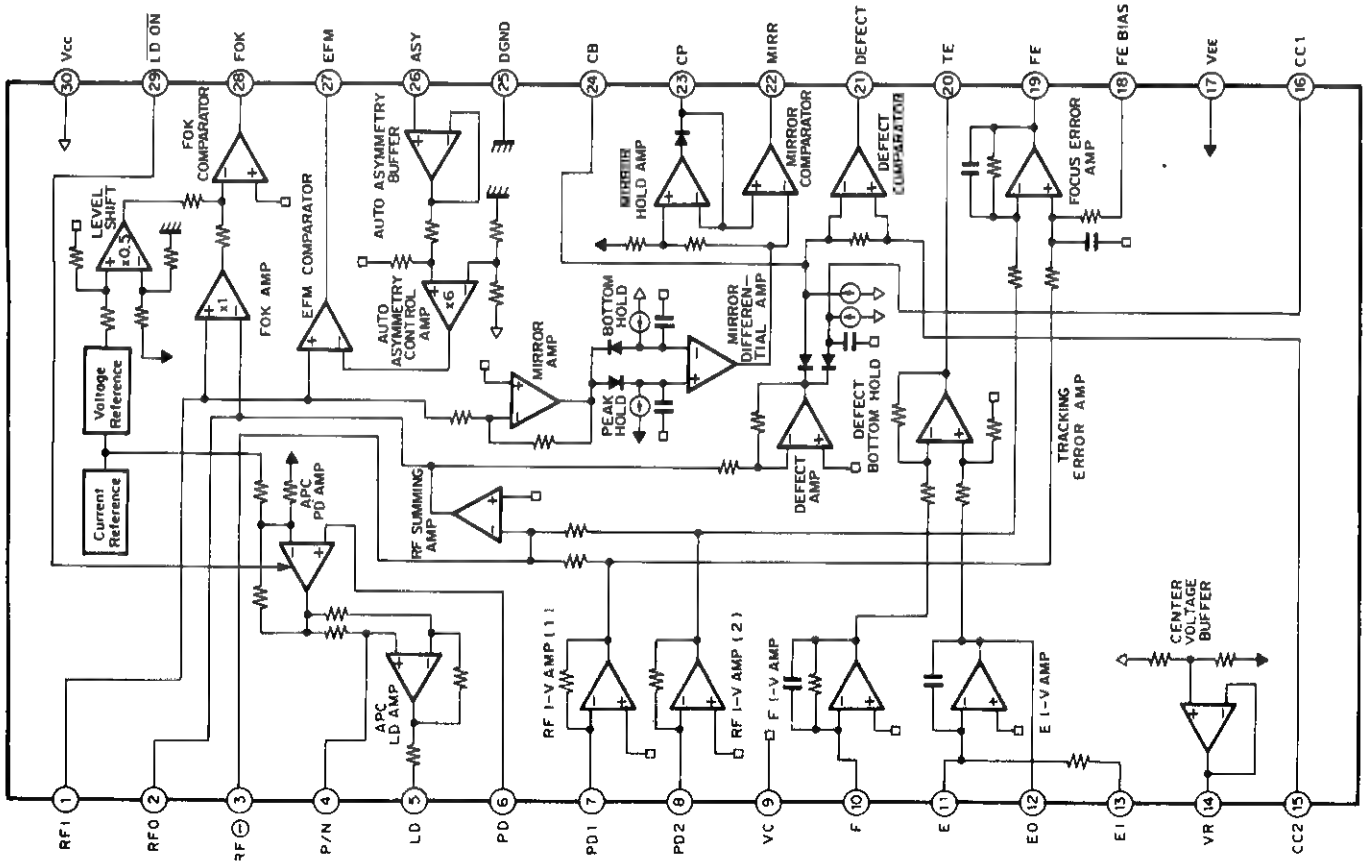


Fig.5–1

CIRCUIT DESCRIPTION

5–2. Explanation of terminals (V_{CC}= 2.5V, V_{EE}= D_{GND}= –2.5V, VC= GND)

Terminal No.	Terminal name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode) (DC voltage: in N-sub mode)
5	LD	O	–1.8	*APC LD amplifier output pin (DC voltage: PD open in N-sub mode)
6	PD	I	0	*APC LD amplifier input pin. (DC voltage: open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin Current input by connecting to the photodiode A+C terminal.
8	PD2	I	0	RF I-V amplifier (2) inverted input pin. Current input by connecting to the photodiode B+D terminal
9	VC	–	0	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	0	F I-V amplifier inverted input pin. Current input by connecting to the photodiode F terminal.
11	E	I	0	E I-V amplifier inverted input pin. Current input by connecting to the photodiode E terminal.
12	EO	O	0	E I-V amplifier output pin
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment
14	VR	O	V_{CVO}	DC voltage output pin of (V_{CC}+V_{EE})/2.
15	CC2	I	1 0	Input pin for the C-coupled signal output from the defect bottom hold.
16	CC1	O	1 2	Defect bottom hold output pin.
17	V_{EE}	–	–2.5	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	0	Bias pin on the focus error amplifier non-inverted side. For CMR adjustment of the focus error amplifier.
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin. (DC voltage: connected to a 10 k-ohm load).
22	MIRR	O	V_{MIRL}	Mirror comparator output pin. (DC voltage: connected to a 10 k-ohm load).
23	CP	I	–1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin.
25	DGND	–	–2.5	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	–	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin (DC voltage: connected to a 10 k-ohm load)
28	FOK	O	V_{FOKL}	FOK comparator output pin. (DC voltage: connected to a 10 k-ohm load).
29	LD ON	I	–2.5 (DGND)	LD ON/OFF select pin. (DC voltage: when LD ON)
30	V_{CC}	–	2.5	Positive power supply.

*APC Automatic Power Control

Table 5–1

CIRCUIT DESCRIPTION

5–3. Function explanation

● RF amplifier

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58 k-ohms in RF I-V amplifier (1) and (2) respectively.

The voltage which is converted from the current of the photodiode (A+B+C+D) is added in the RF summing amplifier and is output from the RFO pin. The eye pattern can be checked at this pin.

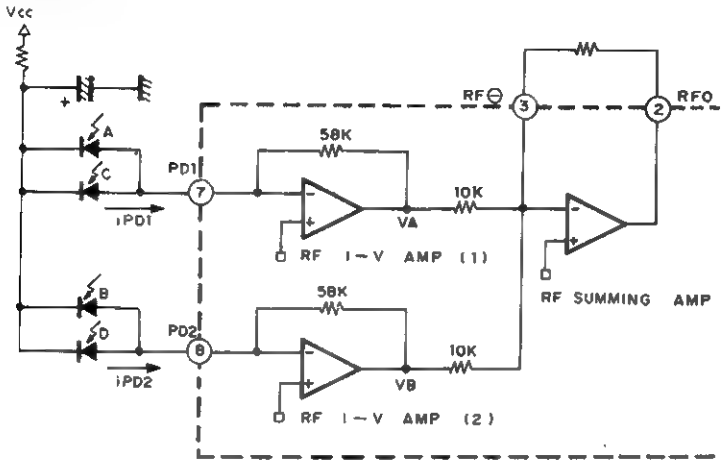


Fig. 5–2 RF I-V AMPLIFIER

The ow frequency component of the RFO output voltage, V_{RFO} s represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6 \text{ k-ohms} \times (I_{PD1} + I_{PD2})$$

● Focus error amplifier

The difference between the RF I-V amplifier (1) output (VA) and the RF I-V ampl fier (2) output (VB) is calculated, and the current of the photodiode (A+C−B−D) is converted to a voltage and output.

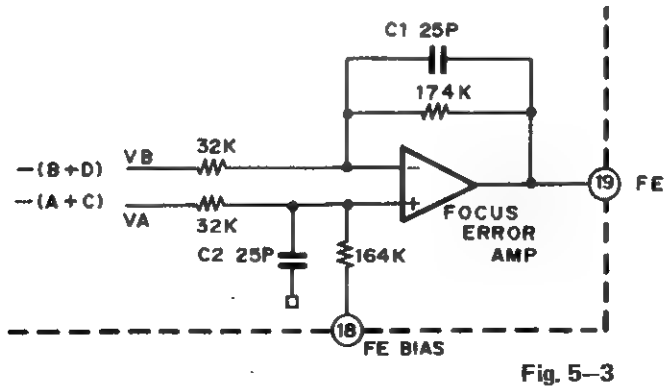


Fig. 5–3

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (I_{PD2} - I_{PD1}) \times 315.4 \text{ k-ohms}$$

The common mode rejection ratio of the VR connected to pin ⑱ is maximized when the composite impedance to GND is around 10 k ohms (with a VR resistance of around 40 k ohms).

CIRCUIT DESCRIPTION

- **Tracking error amplifier**

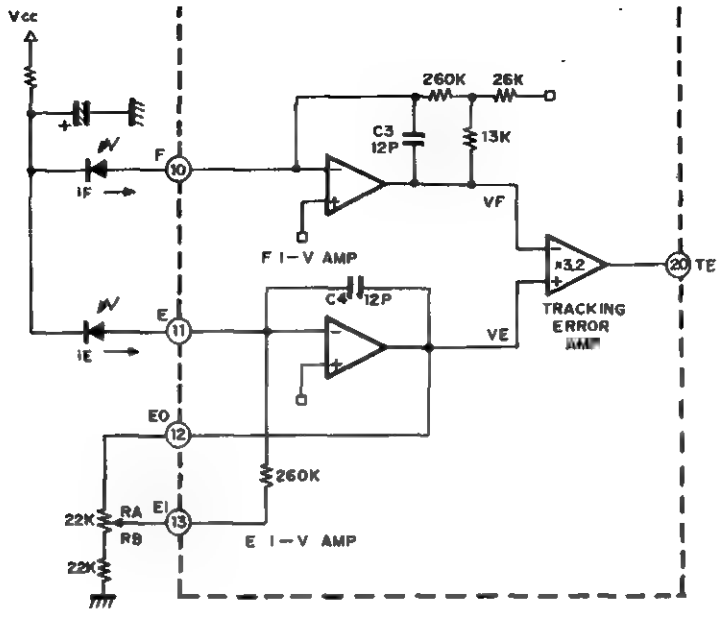


Fig. 5–4

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I-V amplifier and F I-V amplifier respectively.
That is:

$V_F = iF \times 403$ k-ohms

$V_E = iE \times 260$ k-ohms $\times R_A/(R_B + 22\ k) + (R_A + 260\ k)$

The difference between the E I-V amplifier and the F I-V amplifier is calculated by the tracking error amplifier, and the photodiode (E-F) current is converted to a voltage and output.

$V_{TE} = (V_E - V_F) \times 3.2$

$= (iE - iF) \times 1290$ k-ohms

- **Focus OK circuit**

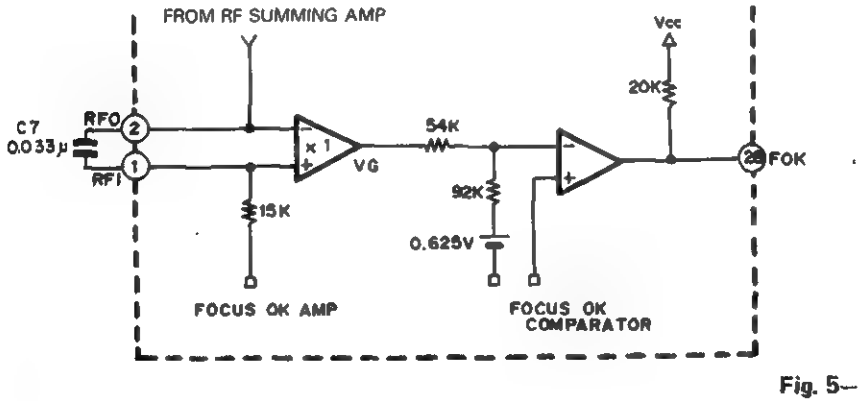


Fig. 5–5

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.
While an RF signal is present at pin ②, an HPF output is present at pin ①. At the same time, the LPF output (opposite phase) of the focus OK amplifier is obtained.
The focus OK output is inverted when $V_{RFI} - V_{RFO}$ is almost equal to −0.37 V

C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amplifier. Normally, C7 = 0.033μF is selected, with fc = 1 kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.

CIRCUIT DESCRIPTION

● Mirror circuit

In the mirror circuit, after the RFI signal is amplified, both its peak and bottom are held.

While the peak hold is held by a time constant which can follow a traverse of 30 kHz, the bottom hold is held by a time constant which can follow a cycle period envelope variation

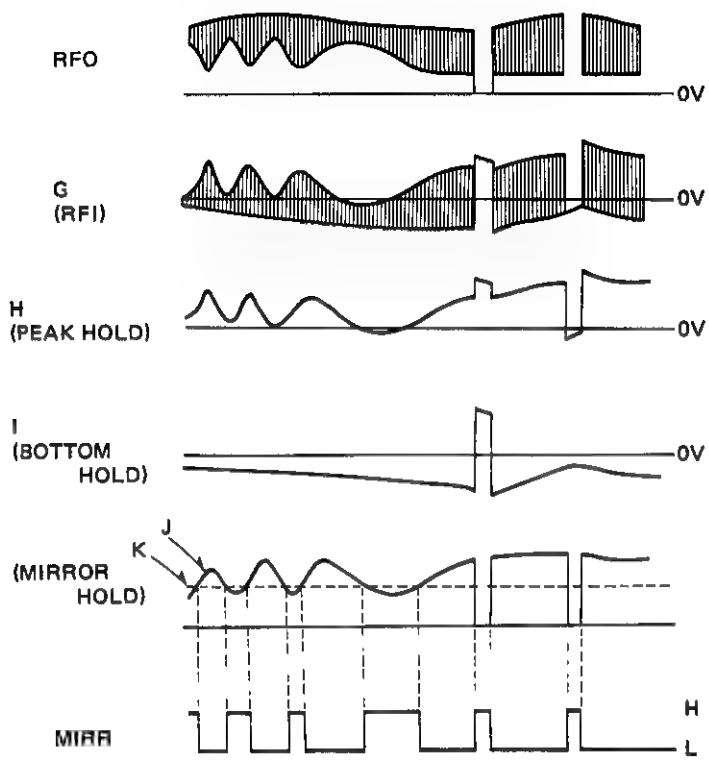


Fig. 5–6

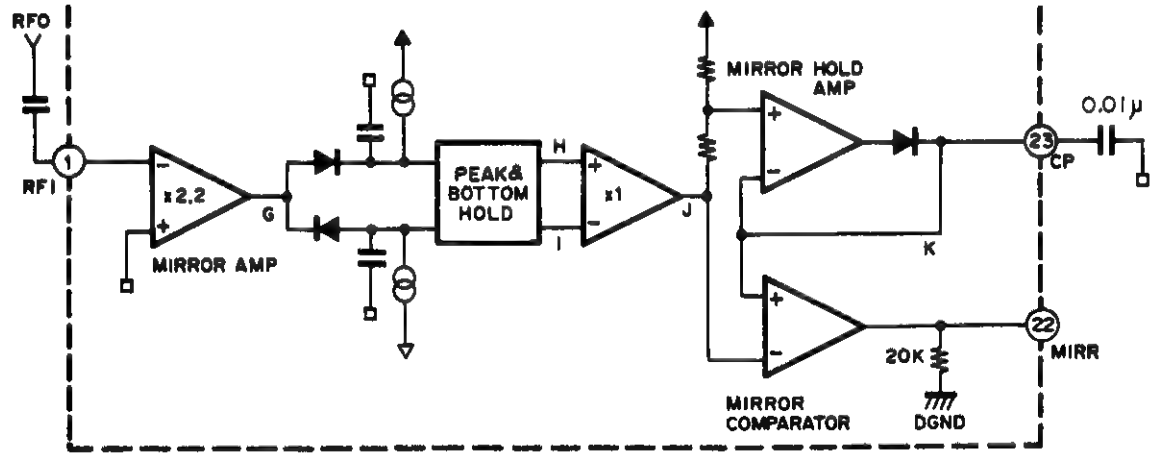


Fig. 5–7

These peak and bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J. This signal is compared with signal K, which is obtained by a peak hold with a large time constant corresponding to 2/3 of the peak value, so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite large when compared with the traverse signal

CIRCUIT DESCRIPTION

• EFM comparator

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristic that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal

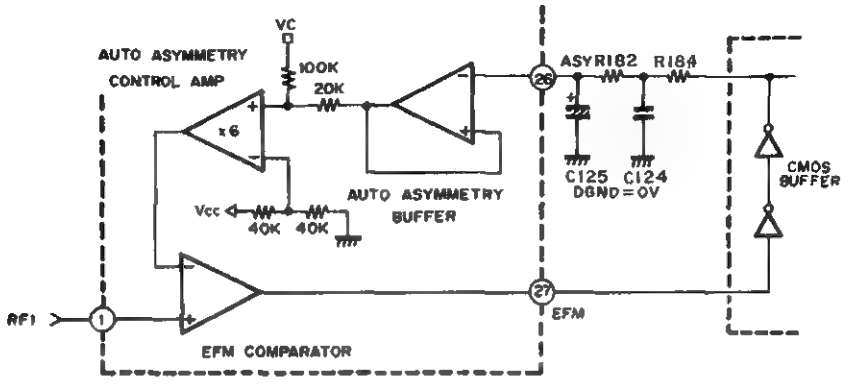


Fig. 5–8

The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer. R182, R184, C124 and C125 constitute an LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.

• Defect circuit

After inverting the RFI signal, the defect circuit bottom holds with two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1 msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generate the mirror defect detecting signals.

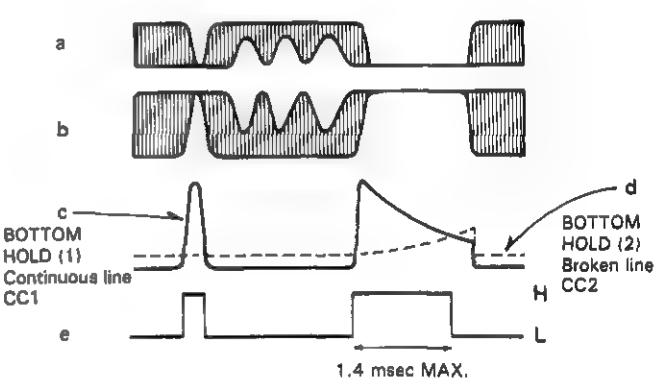


Fig. 5–9

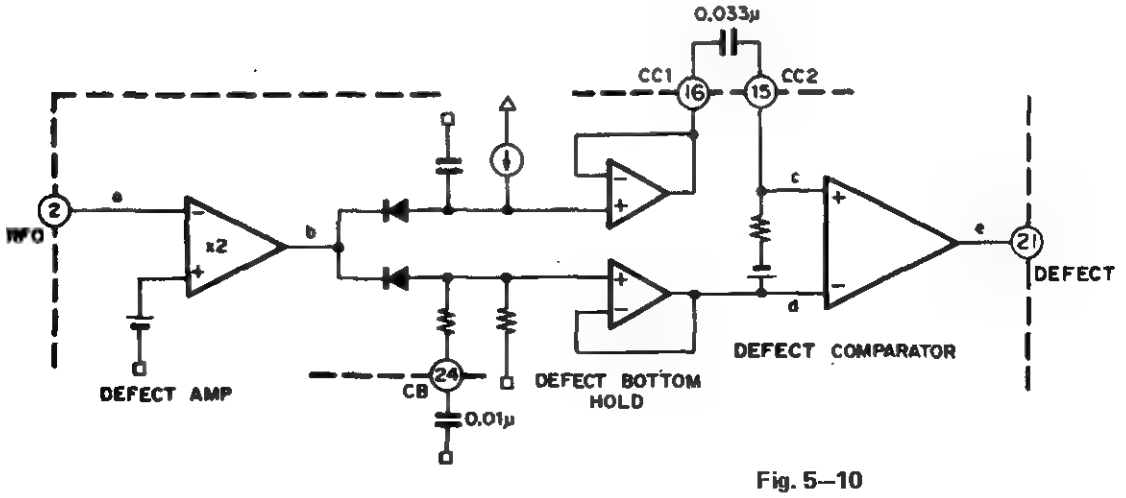


Fig. 5–10

CIRCUIT DESCRIPTION

6. Servo control CXA1244S (X25-331X-XX : IC6)

CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- Focus control (search ON/OFF, gain control)
- Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CX23035.

6–1. Terminal connection diagram

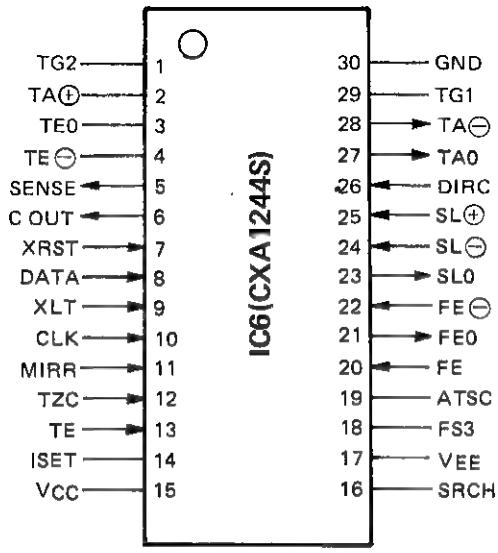


Fig. 6–1

6–2. Block diagram

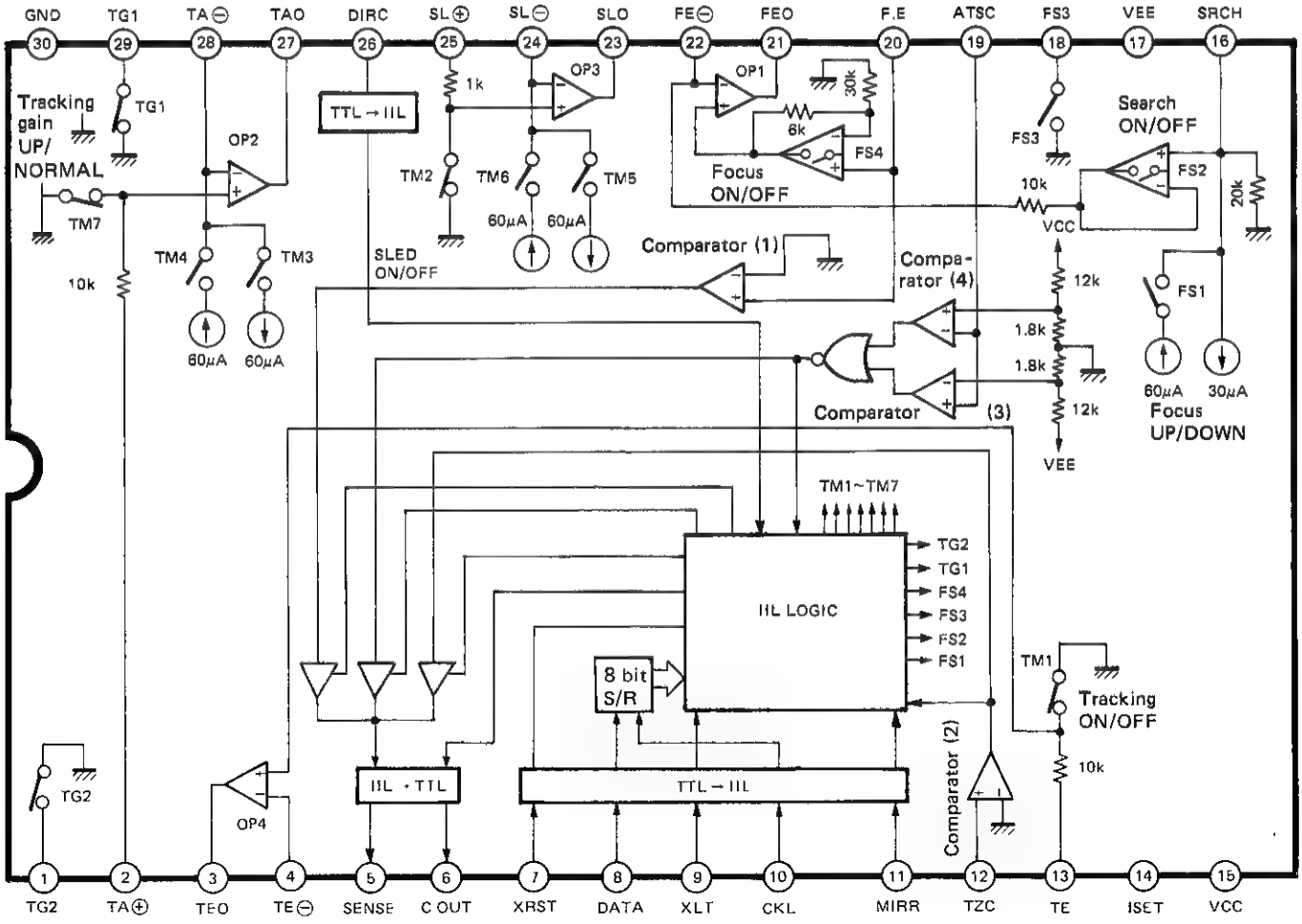


Fig. 6–2

CIRCUIT DESCRIPTION

6–3. Explanation of terminals

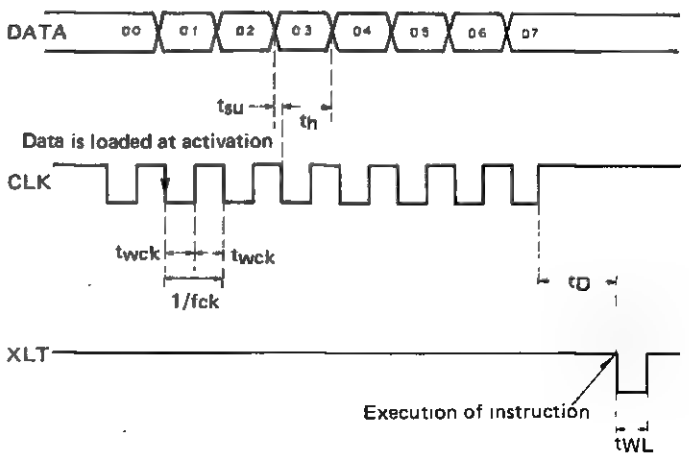
Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally –5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally –5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a trakcing error is input through BPF.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Table 6–1

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus error voltage is 0V or higher. Used at the time of FOCUS PULL opera tion.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%) But this is not used in this equipment
0 0 1 0	TRACKING MODE	TZC	Judgement output of, positive or negative of tracking zero cross, tracking error When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP

Note 2 : Digital unit timing chart



CIRCUIT DESCRIPTION

6–4. System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

Table 6–2

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

CIRCUIT DESCRIPTION

6–5. Serial data truth value table.

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

Table 6–3

TRACKING CONTROL		D2	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

Table 6–4

TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

DC : DIRC input terminal

Table 6–5

CIRCUIT DESCRIPTION

6–6. Explanation of functions

The input data for causing this IC to operate is composed of 8 bits. It is hereinafter expressed in two hexadecimal digits like $XX. (X is 0~F.)

Instructions to CXA1244S are generally divided into three types, i.e., $0X, $1X and $2X. Standard methods for use of these three types are explained below.

- **$0X (⑤ SENSE is "FZC")**

This instruction is related to control of focus servo, and its bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four switches, i.e., FS1~FS4, are what are related to focus, and they correspond to D0~D3 respectively.

1) FS1, FS2 and focus search

The operation of FS1, FS2 is described next. ㉑, ㉒ etc. in Fig. 6–3 indicate terminal numbers of CXA1244S (same hereinafter) OP1 is the operational amplifier for focus servo and the output of FS2 is connected to its inversion terminal. FS2 is such a switch that is ON and works as a usual voltage follower at the time of 1; and that its output is of high impedance at the time of 0. FS1 is a simple current switch which is OFF at the time of 1 and works to allow flow of 60μA at the time of 0. This value of 60μA is what is obtained when 240μA is fed to ISET ⑭ terminal. The voltage for focus search is produced using these FS1, FS2.

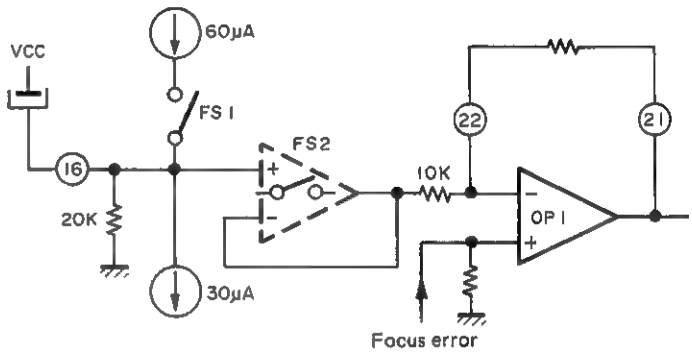


Fig. 6–3 Explanation of FS1, FS2

I $00 ⑯ terminal is charged to (60μA–30μA) x 20kΩ = 0.6V when FS1 = 0. Further, because FS2 = 0, This voltage is not transmitted thereafter, and ouput ㉑ terminal is of 0V.

II $02 FS2 only becomes 1 from the status described above. The output of FS2 is + 0.6V at this time and a negative output is directed to op2. This voltage level is specified as follows.

$$(60\mu A - 30\mu A) \times 20k\Omega \times \frac{\text{Resistance value between } ㉑ - ㉒}{10k\Omega} \quad \text{..... Expression (1)}$$

↑ At the time of 240μA (⑭)

III $03 FS1 becomes 1 from the status described above and the current source of + 60μA is disconnected. Then, the CR's charge/discharge circuit is formed and the voltage at ⑯ terminal decreases as the time elapses as shown in Fig. 6–4.
This time constant is specified by internal 20kΩ and external condenser C101 22μF.

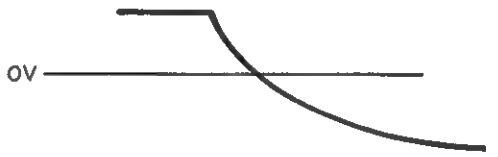


Fig. 6–4 Voltage at ⑯ terminal when FS1 = 0 → 1

It is possible to produce the focus serach voltage by alternately instructing these II and III. (Fig. 6–5)

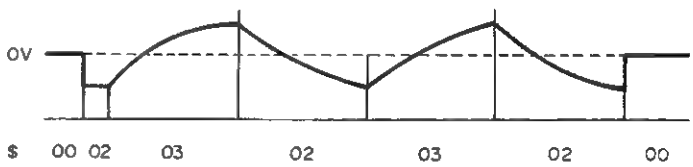


Fig. 6–5 Search voltage is produced by $02 ⇋ $03 (voltage at ⑯ terminal)

CIRCUIT DESCRIPTION

2) Explanation of FS4

This switch is a voltage follower (but the gain is 1.2 times) at the time of 1 and the output is open at the time of 0, like FS2 described earlier. This switch bears focus servo ON/OFF as located between focus error input 20 and input of OP1 described earlier.

$00 → $08

Focus OFF ← Focus ON

3) Focusing procedure

The polarity is specified as follows for explanation.

- The lens searches in the direction of far → near to the disc.
- Output voltage (21) changes as negative → positive at this time.
- Further, the S curve of focus changes as shown in Fig. 6–6.

Focus servo is applied with point Ⓐ shown in Fig. 6–6 as the actuation point. In general, the time when focus search is made and the focus servo switch is ON during passage through point Ⓐ . Furthermore, ANDing is made with focus OK signal (FOK) in order to prevent maloperation.

This IC is of such a design that what is obtained by comparing the focus error with 0V is output out of SENSE (5) terminal as the signal passing through point Ⓐ and is named as FZC (Focus Zero Cross).

Focus OK means a signal that indicates that focus is applied (may be applied, in this case), and it is output out of (28) terminal of head amplifier IC1 (CXA1081M) in X29-1890-00.

when the above description is summarized, focus is applied in accordance with a tim chart like what is shown in Fig. 6–7.

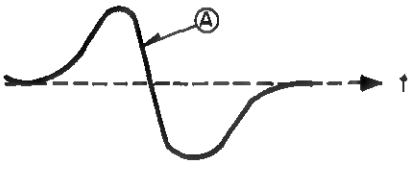


Fig. 6–6 S curve

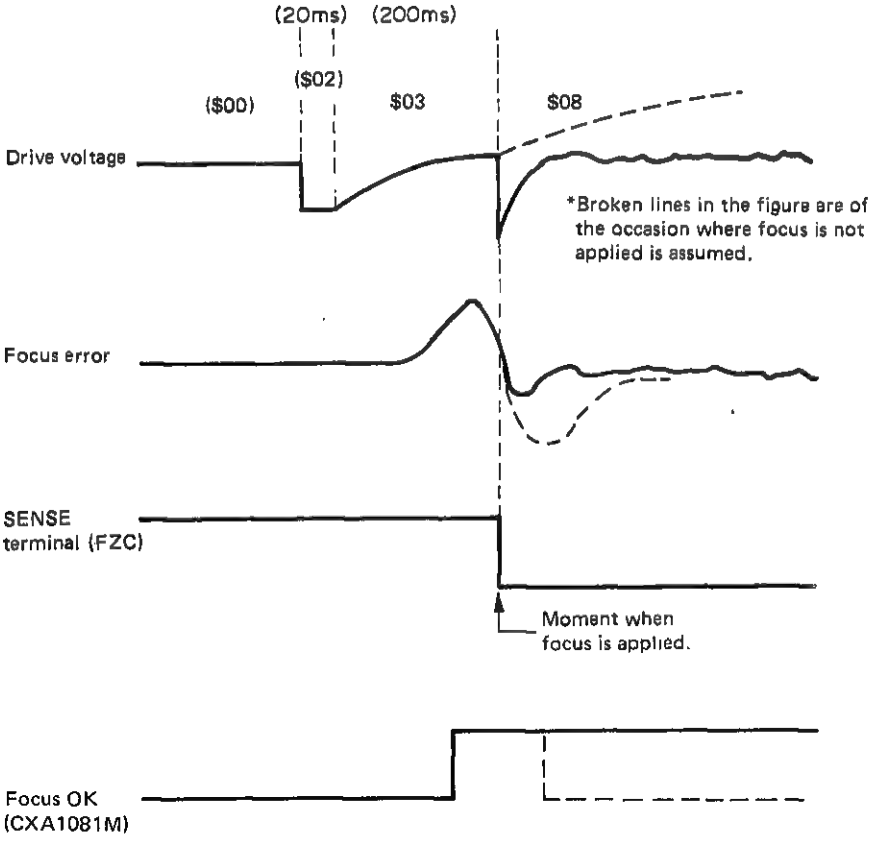


Fig. 6–7 Timing chart of focus OK

CIRCUIT DESCRIPTION

4) SENSE ⑤ terminal

As the output type is open collector of an NPN transistor, it is used with 22kΩ pull up. What is output varies by the input data. That is,

- ○FZC with $0X
- ○"H" when the absolute value of the voltage applied to AS terminal exceeds 0.65V, or "L" when it is up to 0.65V, with $1X.
- ○TZC with $2X

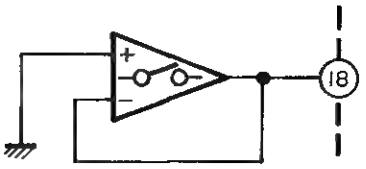


Fig. 6–8 FS3

5) FS3 switch

The type of this switch as shown in Fig. 6–8. It is of GND when FS3 is 1 or is of high impedance when FS3 is 0. See "Method for use of FS3" in the explanation of circuit operation.

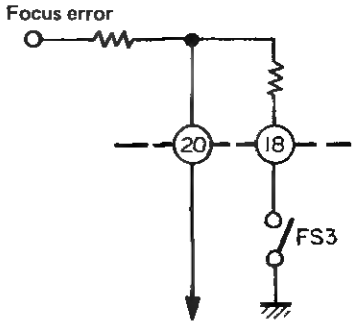


Fig. 6–9 Typical use of FS3

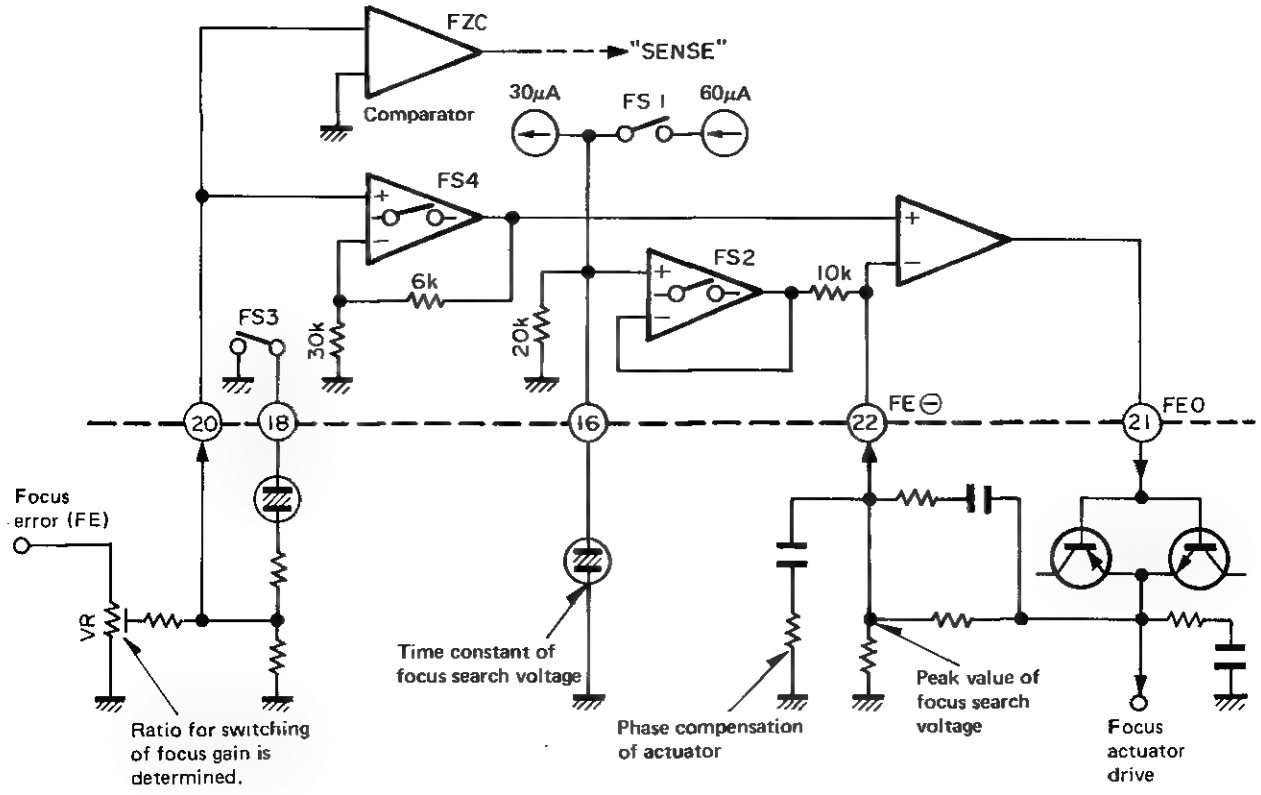


Fig. 6–10

CIRCUIT DESCRIPTION

- **$1X (⑤ SENSE is "AS")**

This instruction is related to TG1, TG2 and brake circuit ON/OFF. The bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1		Brake circuit ON/OFF	TG2	TG1

1) TG1, TG2

The circuit type of these switches is same as that of FS3 shown in Fig. 6–8. However, the logic is opposite. High impedance is obtained with 1, and GND level is obtained with 0. The purpose of the switch is switching between UP/NORMAL of the tracking servo gain. One switch is used for switching of the gain and another for switching of the phase. A typical circuit is shown in Fig. 6–12.

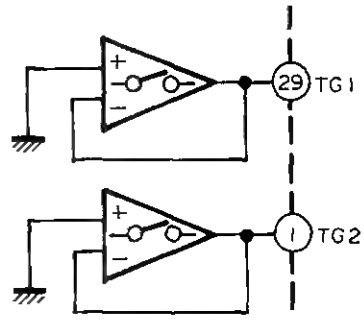


Fig. 6–11 TG1, TG2

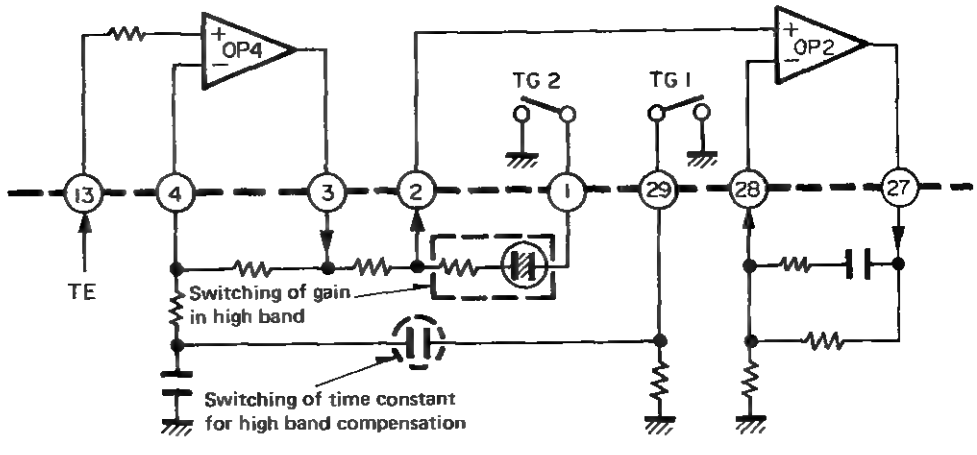


Fig. 6–12 Typical use of TG1, TG2

CIRCUIT DESCRIPTION

2) Brake circuit

The brake circuit is OFF (TM7 is open) when D2 = 0.

The brake circuit is ON (TM7 is open) when D2 = 1.

The brake circuit is explained next. See the section of 100 track jump and 10 track jump as for when the brake circuit is used.

The brake circuit is provided for preventing occurrence of such a phanomenon that only 10 tracks were jumped, even if it was intended to jump 100 tracks, due to the fact that setting of the actuator is exteremely inferior because the servo circuit exceeds the linear range after 100 track jump or 10 track jump. The phase relation between RF's envelope and tracking error is deviated by 180 degrees between the case where the actuator runs across tracks in the radial direction outward and the case where the same runs inward. The unnecessary portion of the tracking error is cut and brake is applied by making use of this nature, for improving setting of the actuator after track jump.

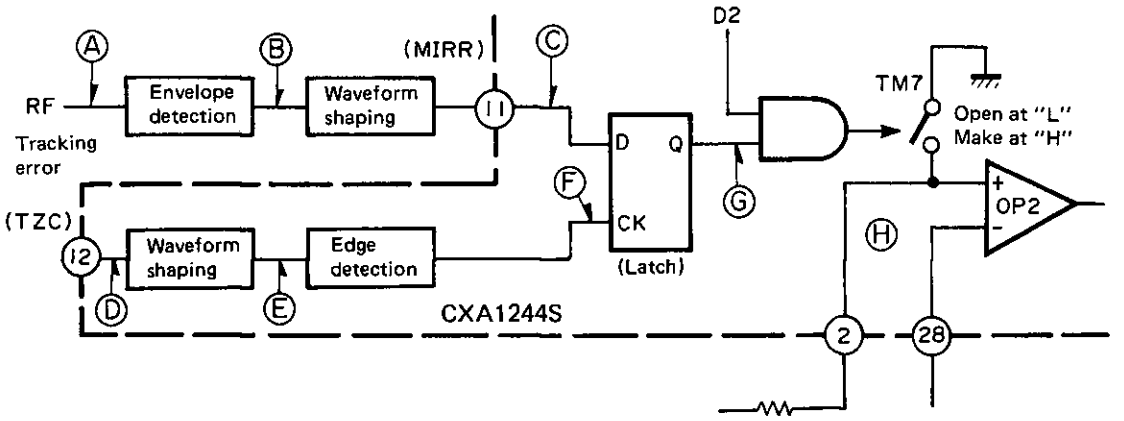


Fig. 6–13 Motion of TM7 (brake circuit)

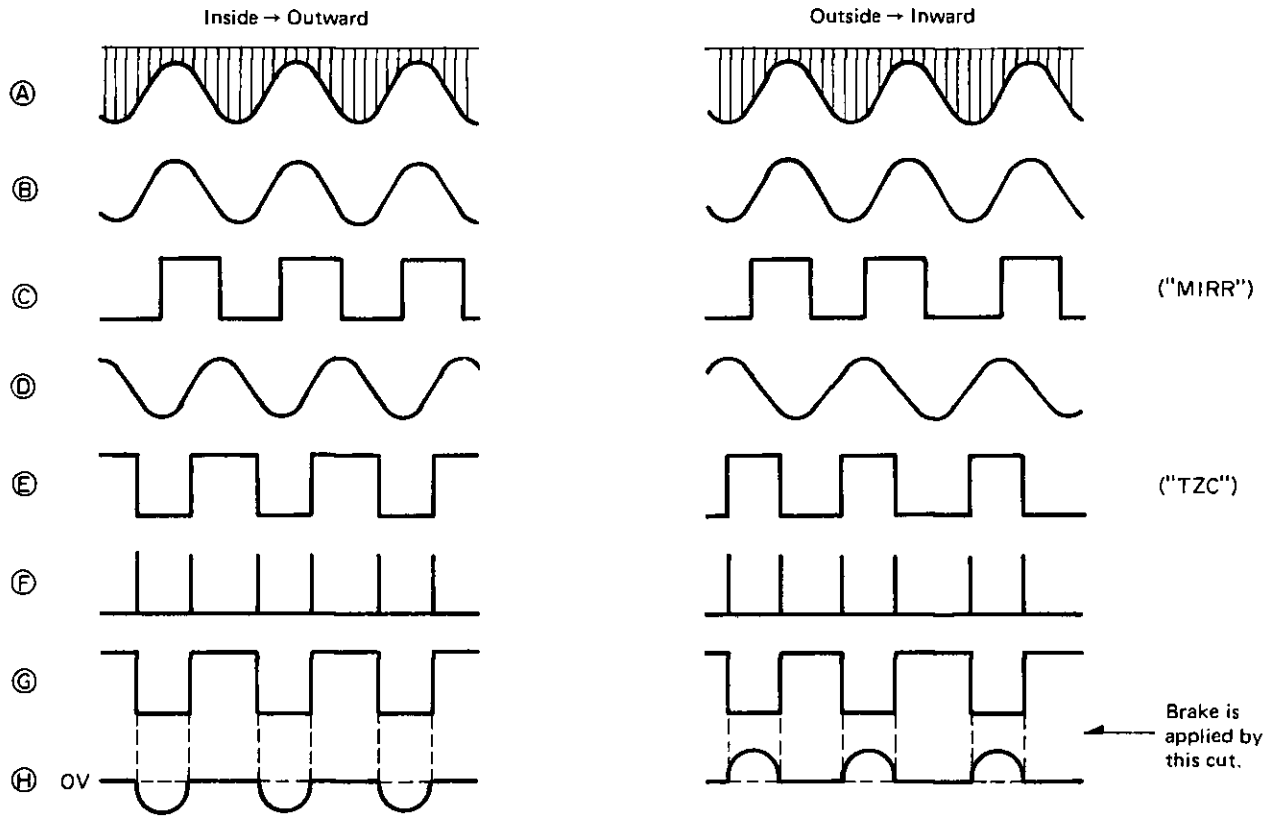


Fig. 6–14 Explanation of Fig. 6–13 (external waveform)

CIRCUIT DESCRIPTION

- **$2X (⑤ SENSE is "TZC")**

This instruction is related to production of jump pulse and fast feed pulse at the time of ON/OFF of tracking servo and sled servo and also at the time of access.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	Tracking control		Sled control	
				00 : OFF		00 : OFF	
				01 : Servo ON		01 . Servo ON	
				10 . F-jump		10 : F-Fast feed	
				11 : R-jump		11 : R-Fast feed	
				⇩		⇩	
				TM1, TM3, TM4		TM2, TM5, TM6	

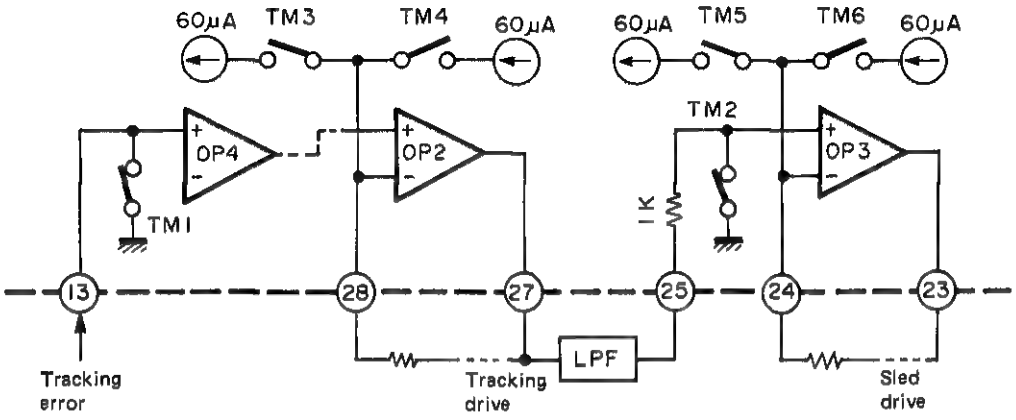


Fig. 6–15 TM1 ~ TM7

The circuit composition is shown in Fig. 6–15. TM1, TM2 make servo ON/OFF, and TM3~TM6 produce jump pulse and fast feed pulse. See truth value table for details.

Figure 60μA is observed in Fig. 6–15. This value is of the case where 240μA is fed to ISET ⑭ terminal like SF1. The circuit of ⑭ terminal is as shown in Fig. 6–16. Therefore, the potential is around (–)VEE + 0.9V.

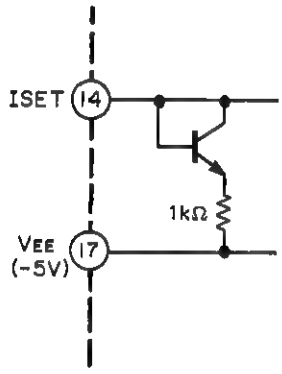


Fig. 6–16 ISET terminal

1) DIRC ㉖ terminal and single track jump

1 track jump usually gives an acceleration pulse, and then observes the tracking error; gives deceleration pulses for a fixed length of time from the time when the tracking error ran across 0 point, and again turns ON the tracking servo. 100 track jump to be explained in the next paragraph is satisfactory if approximately 100 tracks are jumped, but 1 track jump should be absolutely 1 track jump. Therefore, such a complicated measure is taken.

Therefore, DIRC (Direct Control) terminal is provided for this IC in order to facilitate single track jump by its operation. That is, for performing single track jump using DIRC (DIRC is usually "H")

- ○An acceleration pulse is produced. ($2C if REV; or $28 if FWD)
- ○DIRC is changed to "L" by TZC ↓ (or TZC ↑). (⑤ SENSE is "TZC".) The polarity of the jump pulse is inverted and deceleration is applied.
- ○DIRC is changed to "H" after a fixed length of time. Both tracking servo and sled servo are ON automatically.

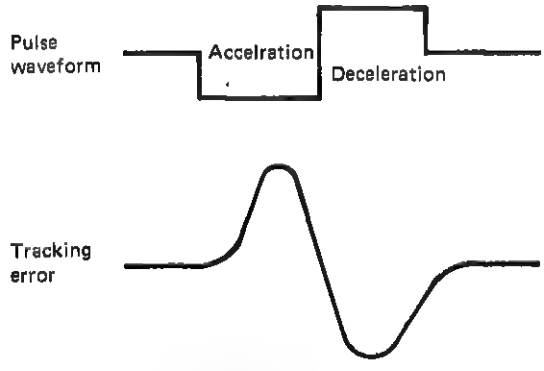


Fig. 6–17 Pulse waveform and tracking error of signal track jump

CIRCUIT DESCRIPTION

2) 100 track jump

With this IC, basically it is not possible to change the amplitude of the jump pulse between 1 track jump and 100 track jump. (Because the value of the current input to ISET ⑭ terminal is fixed.)

Therefore, the amplitude is determined by 1 track jump and 100 track jump is controlled by time with the voltage remaining unchanged.

100 track jump is of smooth feed by jointly using sled fast feed (so-called "kick-off") besides drive of the tracking actuator. The length of this kick off is determined so that the access time is the minimum.

Brake circuit ON and tracking gain UP are made to stabilize the setting operation after the jump.

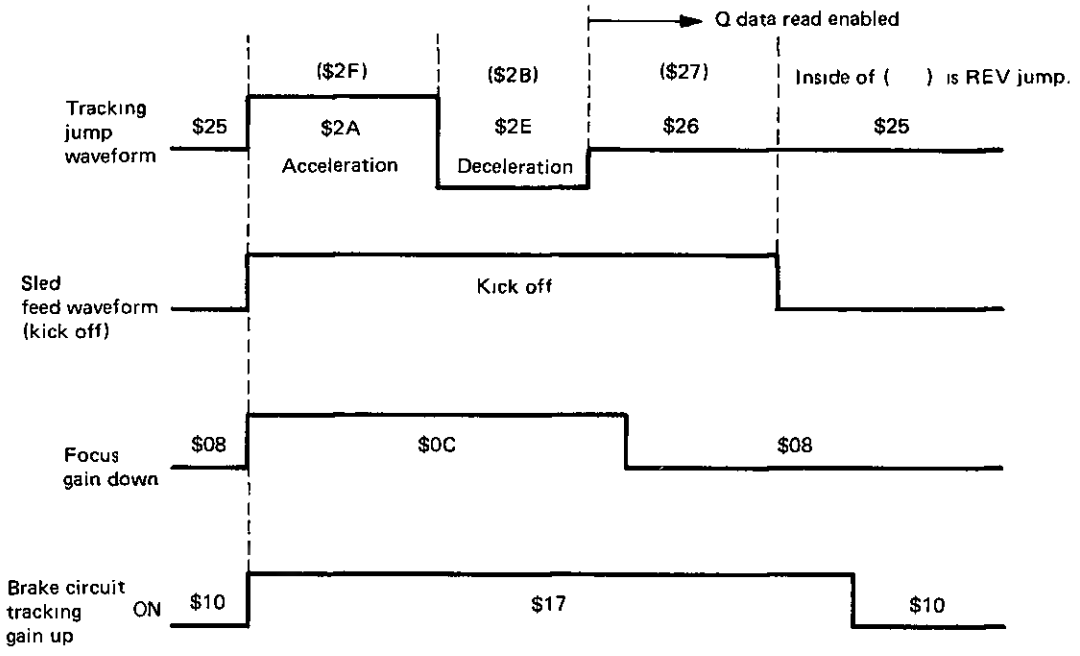
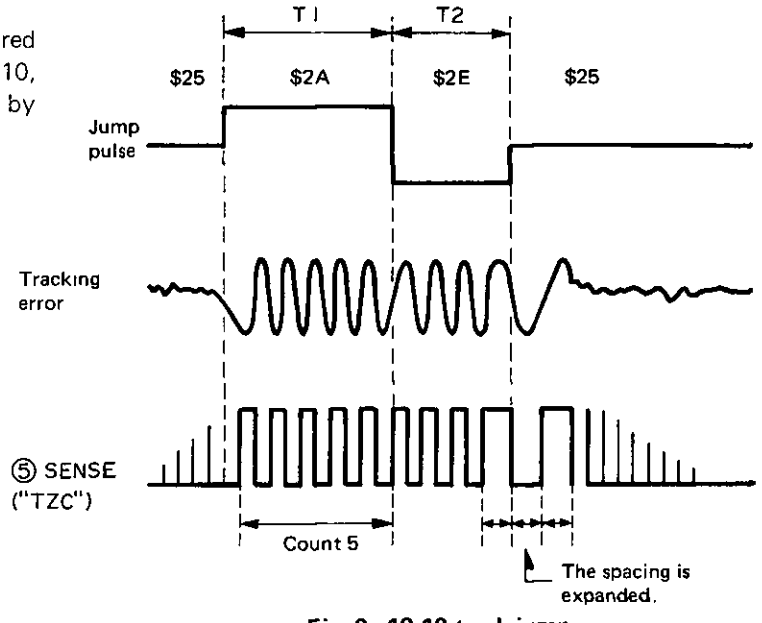


Fig. 6–18 100 track jump timing chart

3) 10 track jump

As this is intermediate between 100 and 1, the required number of tracks is set at a value that is close to 10, and therefore, the jump pulse width is determined by counting the number of jumped tracks.



Acceleration time T1 : Five TZCs are counted.
Deceleration time T2 : Expansion of spacing between TZCs is detected. (Max. time setting)

Fig. 6–19 10 track jump

CIRCUIT DESCRIPTION

4) Access by making joint use of 100, 10 and 1 track jumps

Jump pulses and kick off pulses (that is, $2X relaiton) are set as described in the paragraph of $2X and subsequent, and as for $1X relation, instructions are output in a batch.

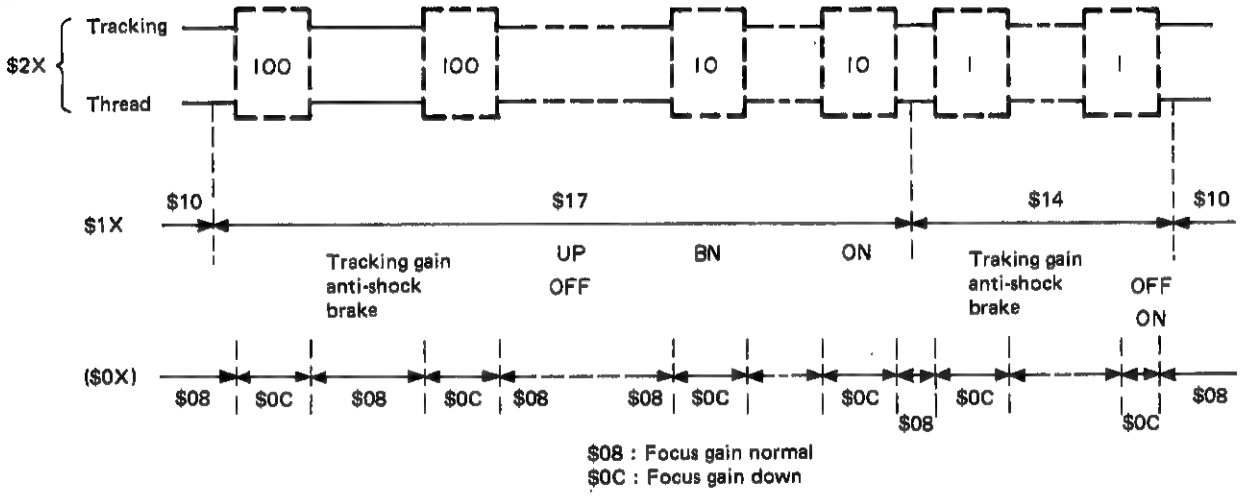


Fig. 6–20 Typical access time instruction codes

- **How to use high speed access and Count Out ⑥**

It is needless to say that access time for head search of a music and so forth is shorter. In the access using 100, 10, 1 track jump, however, about 4 seconds is the limit from the innermost periphery to the outermost periphery of the disc. It is because 100 track jump consumes more than 80% of the time, and it is possible to shorten the time if the length of time of this "major movement" can be shortened. As the distance from the current location to the destination can be learned from the TOC and the absolute time of the current location, rough feed is made for this distance.

Several methods are available as for the means to replace this distance. In general, it is the number of tracks divided by 1.6μm, sled motor revolution (number of steps, if it is a stepping motor) or potentiometer's voltage, if provided.

C.OUT ⑥ , which is a terminal exclusive for counting number of tracks is provided on this IC in order to make correspondence to counting of number of tracks. As this signal is what is obtained by latching MIRROR signal by the edge of TZC (that is, same as the signal used in the brake circuit), and therefore, even if tracking error signal, etc. include noise, such noise is ignored.

CIRCUIT DESCRIPTION

7. Signal processor CXD1135QZ (X25-331X-XX : IC7)

General

The CXD1135QZ is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter
12. Digital audio interface output

Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

7–1. Block diagram

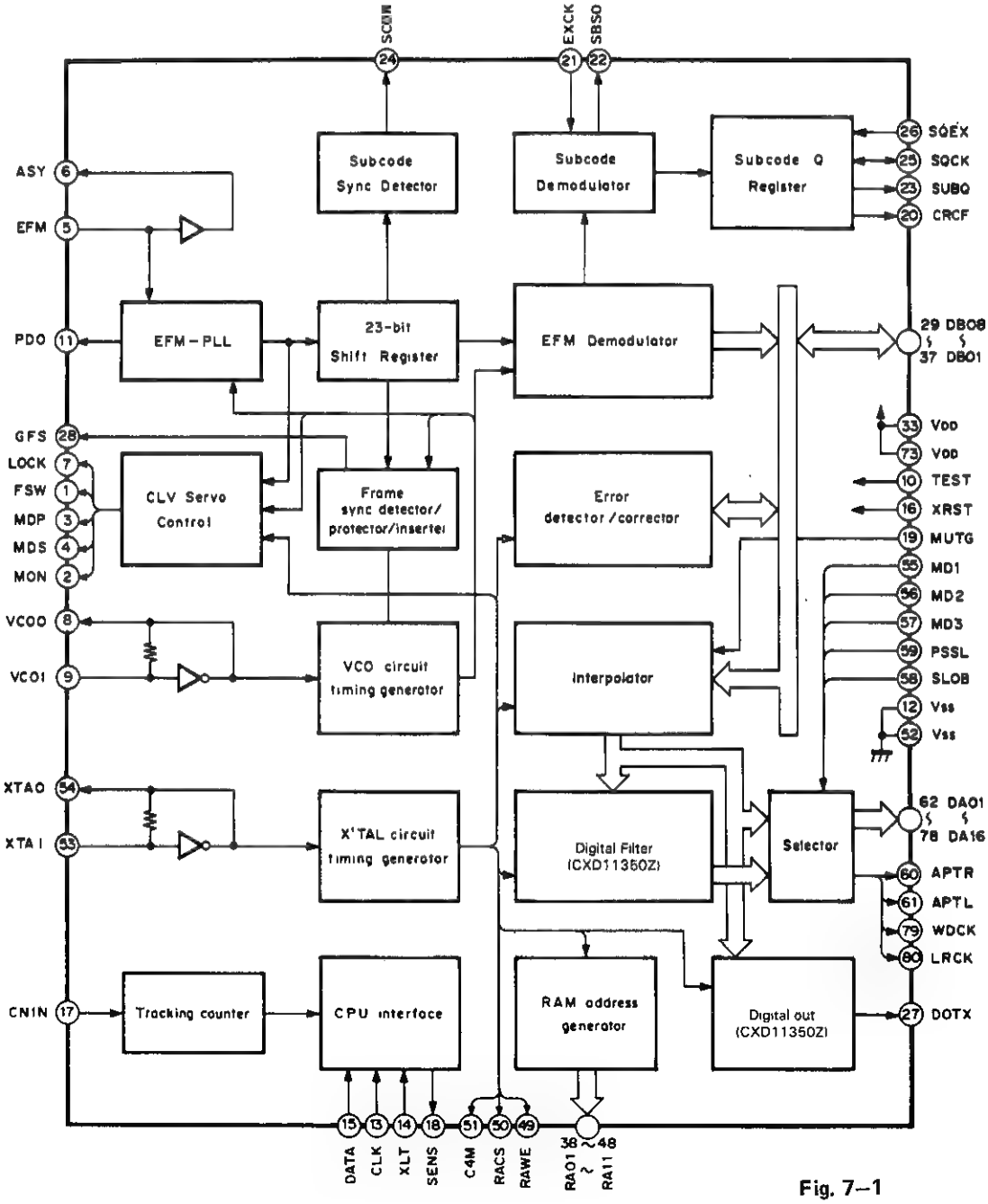


Fig. 7–1

CIRCUIT DESCRIPTION

7–2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L" Normal status when MUTG is "L" or soundless state when it is "H"
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\text{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

Table 7–1

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM ADDR07
45	RA08	O	Address output of external RAM ADDR08
46	RA09	O	Address output of external RAM ADDR09
47	RA10	O	Address output of external RAM ADDR10
48	RA11	O	Address output of external RAM ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f = 4.2336 MHz.
52	V_{SS}	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parale output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L"
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L"
70	DA09	O	DA09 output when PSSL = "H", $\overline{PLCK}$ output when PSSL = "L"
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L"
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	V_{DD}	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{C21O}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C21O output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF.

Table 7–2

Notes:

C1F1 :
C1F2 : Error correction status monitor output for C1 decode.

C2F1 :
C2F2 : Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{PLCK}$: VCO/2 output. f = 4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

$\overline{C21O}$: C21O invert output.

C21O : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

7–3. Explanation of functions

• CPU interface

1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 7–2 at three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 7–3, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

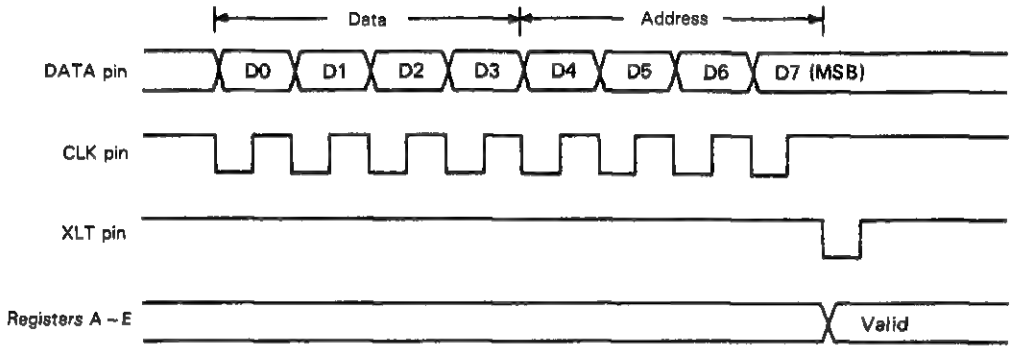


Fig. 7–2 Timing chart for data input

2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 35)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 41)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**11. Countermeasures to defects**". (Page 48)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 46)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB

D1 : WSEL, D2 : GSEL, D3 : GSEM — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 37)

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address.

Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case

CIRCUIT DESCRIPTION

Register E — CLV mode

It is as shown in Table 7–3.

The details of each mode will be described in "**6. CLV servo control**". (Page 41)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data				SENS pin
			D3	D2	D1	D0	
9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A*2	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E*4	CLV mode	1110	CLV mode				$\overline{\text{PW} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4, WFCK/4
		1	RFCK/8, WFCK/8
T_B	D2	0	RFCK/32
		1	RFCK/16
T_P	D1	0	RFCK/4
		1	RFCK/2
GAIN	D0	0	−12 dB
		1	0 dB

Phase comparison frequency in CLV-P mode	
Bottom hold period in CLV-S, CLV-H mode	
Peak hold frequency in CLV-S mode	
Gain at MDP pin in CLV-S, CLV-H mode	

***4 Register E**

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 7–3 List of registers

CIRCUIT DESCRIPTION

3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal (COMPLETE) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal (COUNT) of CNIN/2n (Hz) is output.

The tracking counter timing chart ia shown in Fig. 7–3.

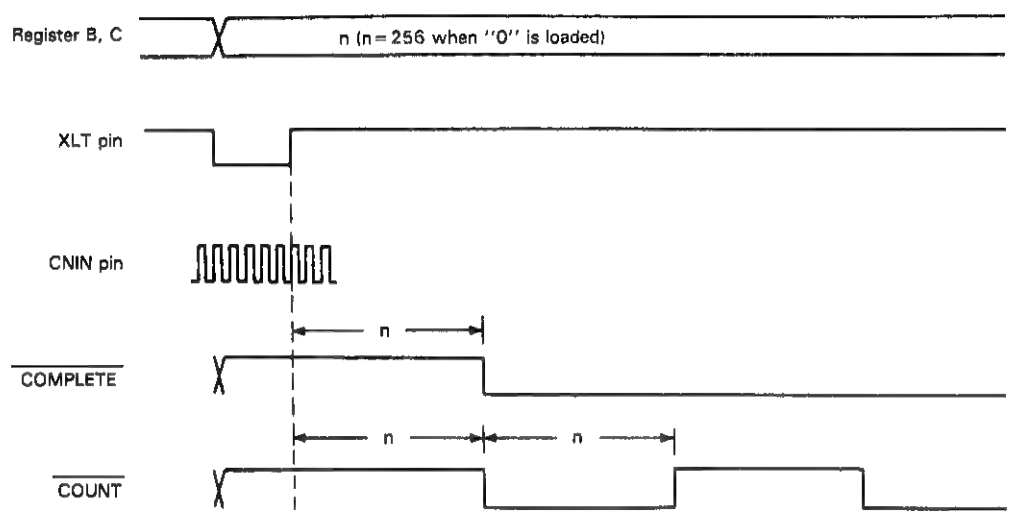


Fig. 7–3 Tracking counter timing chart

4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) COMPLETE : Address (see note) is "B"; Shown in Fig. 9.

(2) COUNT : Address (see note) is "C"; Shown in Fig. 9.

(3) PW≧64 : Address (see note) is "E"; This signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 7–2.

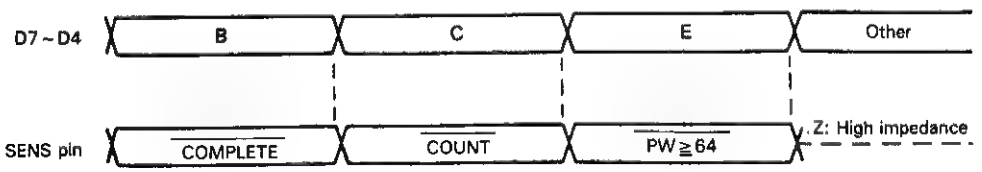


Fig. 7–4 Timing chart of SENS pin

CIRCUIT DESCRIPTION

5) Sub code output

Sub codes P ~ W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0 + S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

b When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80 bit shift registers, for reading and writing, are incorporated as shown in Fig. 7–8 and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

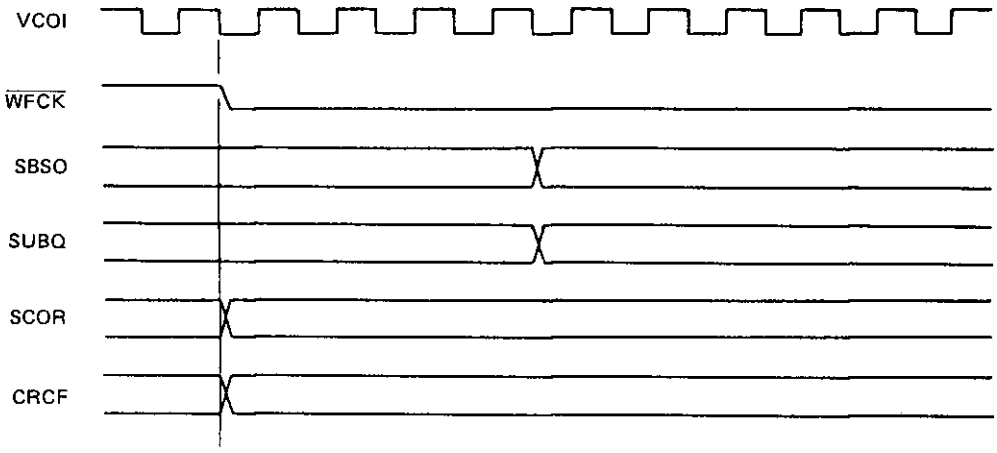
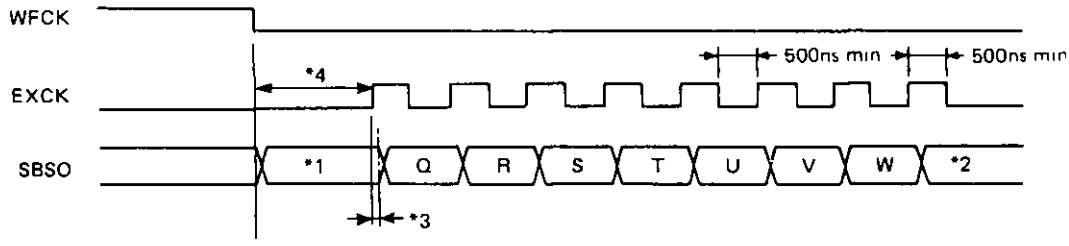


Fig. 7–5

(b) Timing of SBSO, EXCK



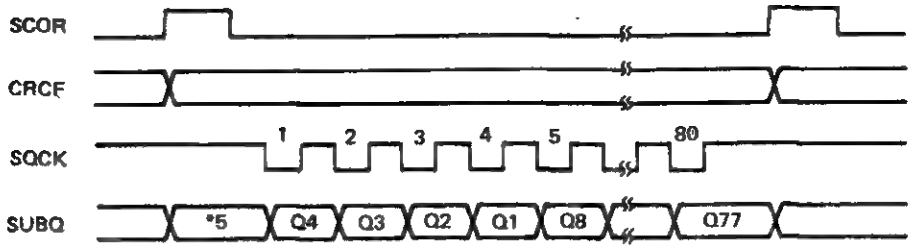
*1: Sub code P is output when SCOR is 0
S0 + S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T ~ 6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T = 8.6436 MHz

Fig. 7–6 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

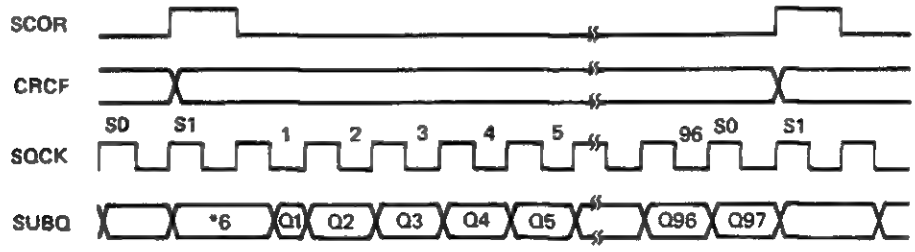
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5: CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6: CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 7–7 Timing chart of sub code outputs

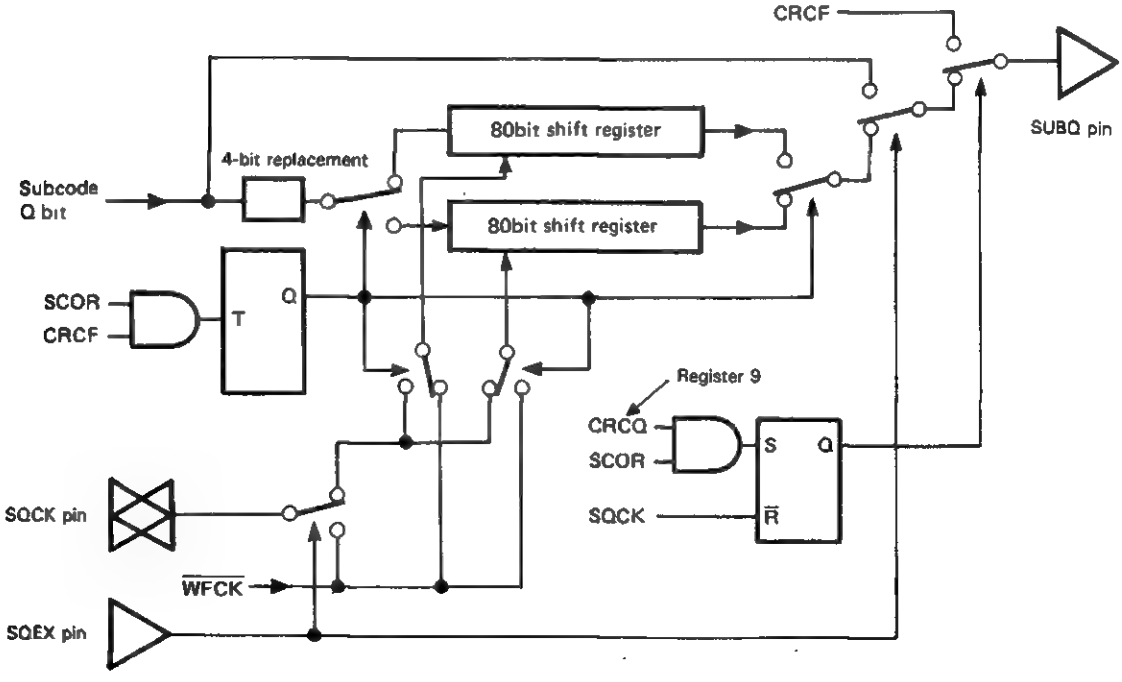


Fig. 7–8

CIRCUIT DESCRIPTION

• EFM demodulation

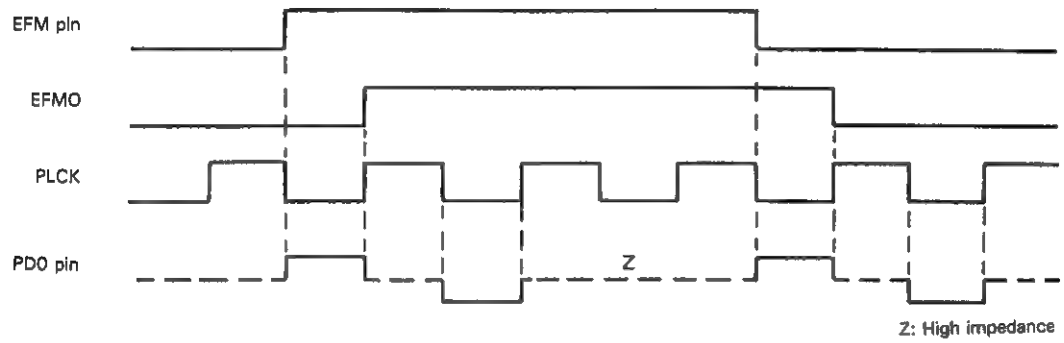
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.

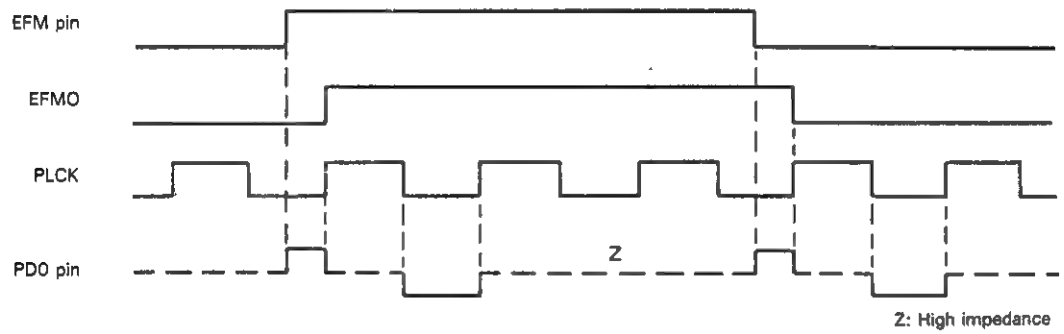
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 7–9.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

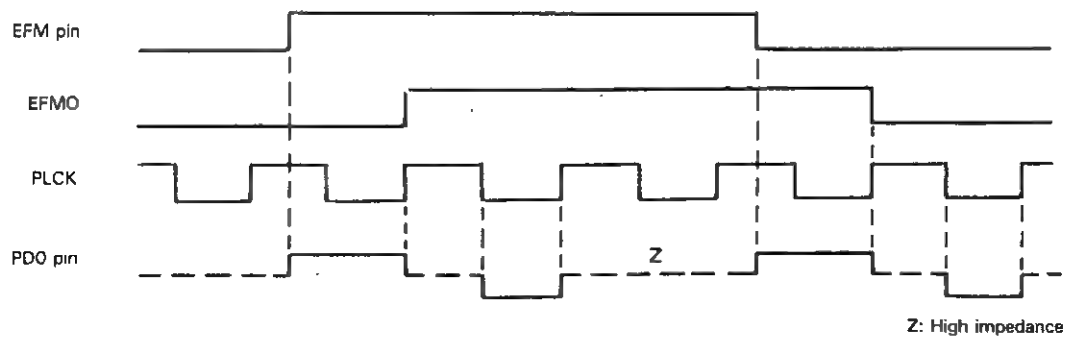


Fig. 7–9 Timing chart of EFM-PLL circuit

CIRCUIT DESCRIPTION

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.

If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 ≒ 7.35 kHz).

A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

• Sub code demodulation

1) Sub code demodulation

Synchronizing signals S0 and S1 of 14 bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).

Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation, and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.

The details of this timing will be shown in **"1. CPU interface"** (Page 32)

2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.

It goes "L" when an error is detected. If the CRCQ flag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**

CIRCUIT DESCRIPTION

- **RAM interface (generation of extermal RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.

This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.

This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.

In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.

The requests from the error correction unit are of the lowest priority among requests of three types.

After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal.

This block generates type address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing.

This interleave processing is subjected to data lag by the unit of a frame.

Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer.

The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

CIRCUIT DESCRIPTION

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.
In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

6) Jitter margin

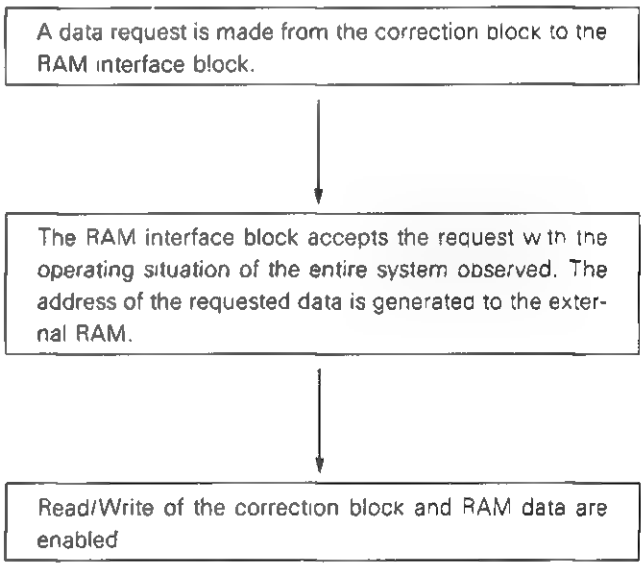
The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.
However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.
In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.
As a result, there is no case where data without error correction is output to the D/A.
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

● Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.
(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bit).
(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
(7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows



(9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to "L" when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

CIRCUIT DESCRIPTION

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

• CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) STOP: Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

(2) KICK: Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

(3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

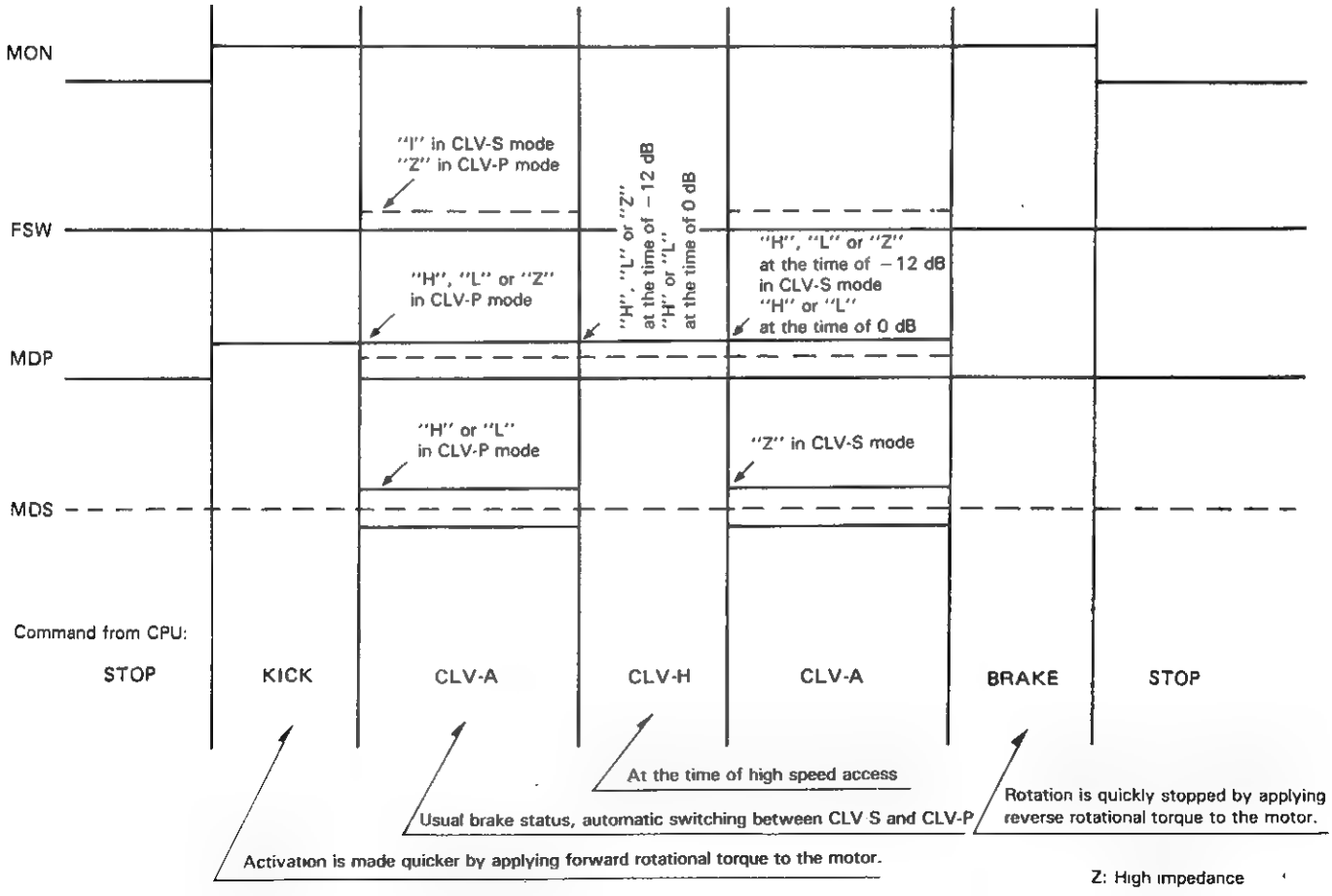


Fig. 7–10 Typical control of spindle motor

CIRCUIT DESCRIPTION

(4) CLV-S: Register E = 1110'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.

When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.

"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B

Rough servo mode used at the time of high-speed access.

Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.

Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8 4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

Pwmdx: Pulse width after bottom hold
TB: Bottom hold period, i.e. RFCK/16 or RFCK/32
Z: High impedance

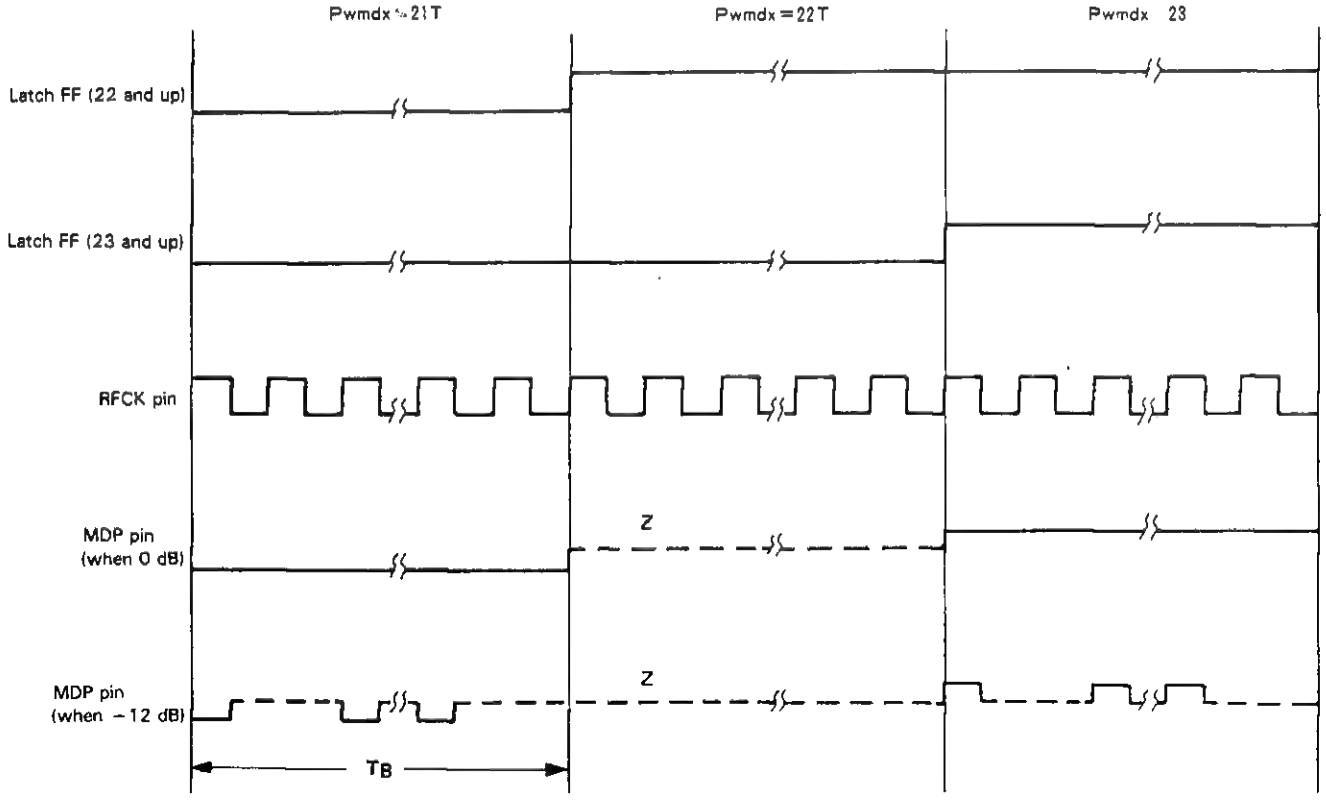


Fig. 7–11 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

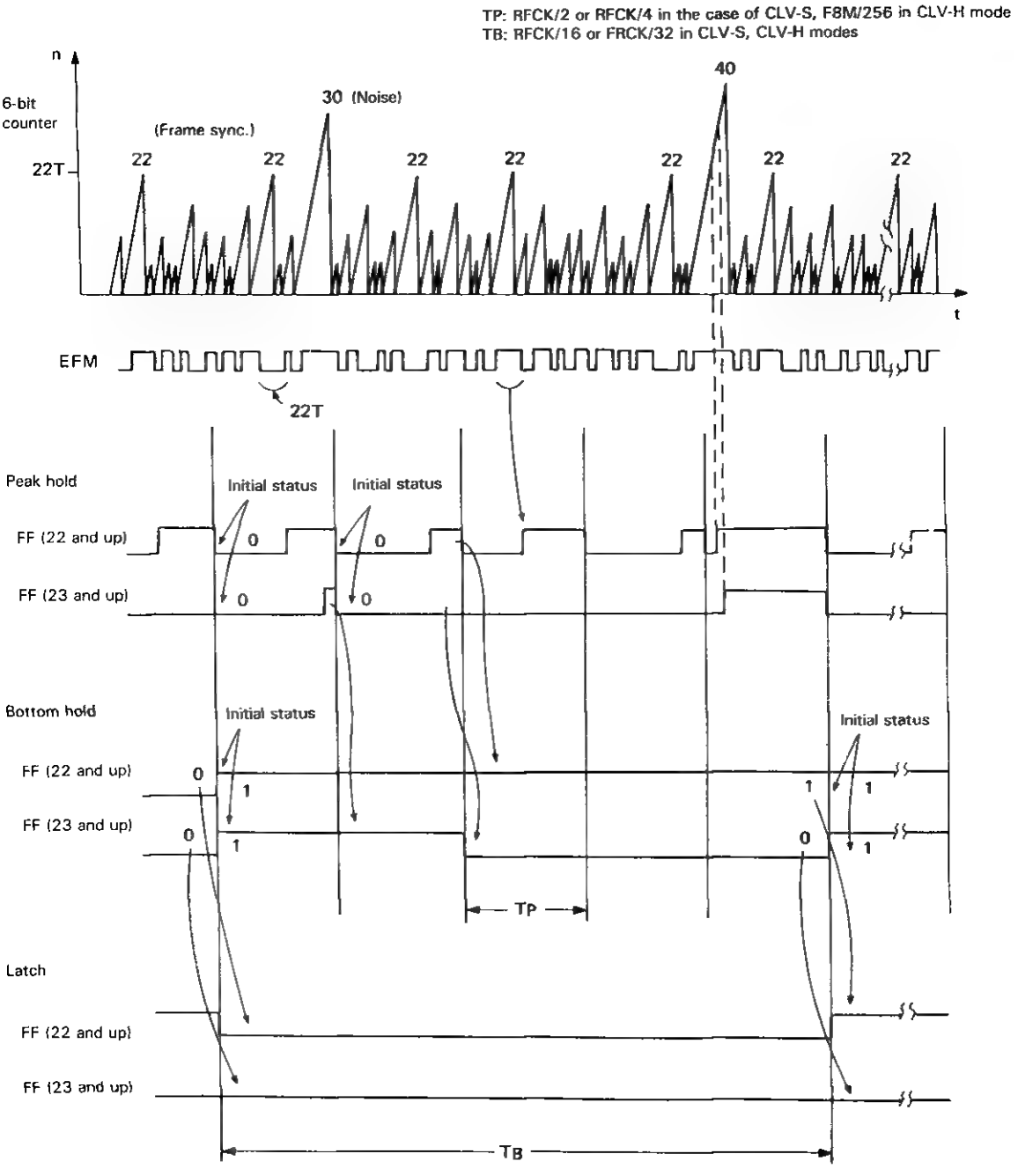
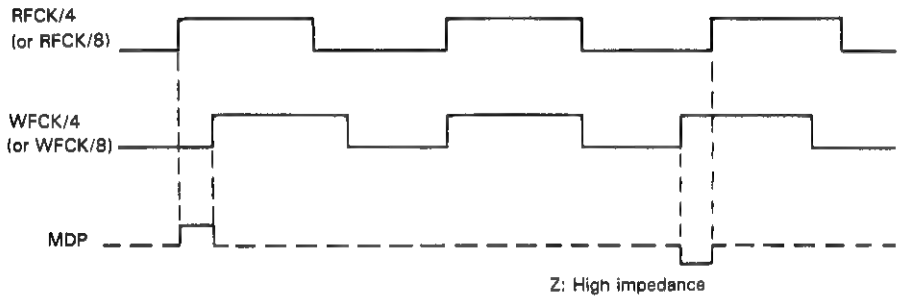


Fig. 7—12 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.
Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (thw 279T) × 32, and then goes "L" until the next trailing edge of WFCK.
MDS = "H" when thw ≧ 279T,
MDS = "L" when thw ≦ 279T
The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ thw ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

MDP pin



MDS pin (The period of 4.2336 MHz is expressed as "T".)

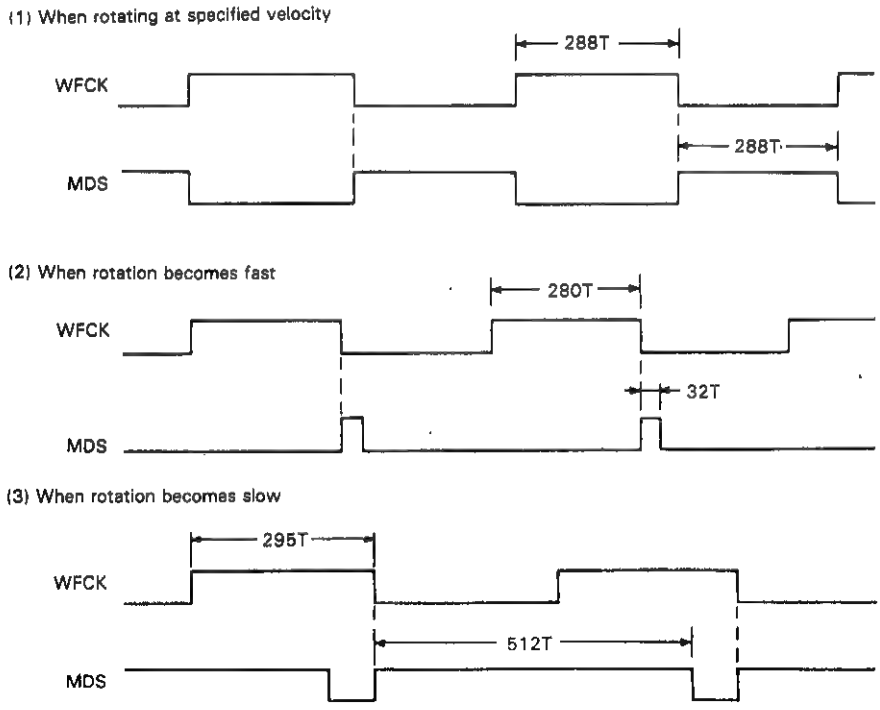


Fig. 7–13 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E = 0110'B

The mode used for normal play status

The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **"1. CPU interface"** (Page 32)

Note:

When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E = 0101'B

New auto servo mode added to the CX23035

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

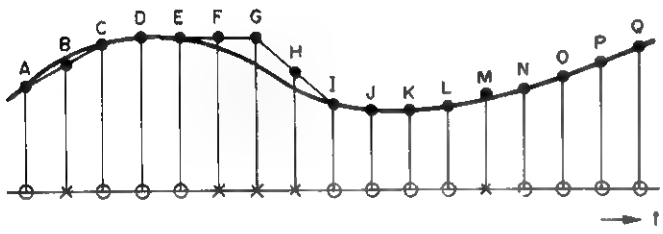
CIRCUIT DESCRIPTION

• Interpolation and mute, attenuate

1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O: Without C2 pointer
X : With C2 pointer

Fig. 7–14

Mean value interpolation

$$B = \frac{1}{2}(A + C)$$

$$H = \frac{1}{2}(E + I)$$: When pointers are continuous

$$M = \frac{1}{2}(L + N)$$

Previous value hold

$$F = G = E$$

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL = H), DA16 (PSSL = L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (-12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higner 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT = "1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	−12 dB	
0	1	$-\infty$ dB	(See Note)
1	1	−12 dB	(See Note)

Note:

When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.

Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

• Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 7–4.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
- **8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz**
- **DO OFF/ON: Digital out OFF/ON**
- **DF OFF/ON: Digital filter OFF/ON**
- **P/S: Parallel output/serial output**
- **OB/2's: Offset binary/2's complement**
- **CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio**

Table 7–4

• Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

• Selection of digital filter (Refer to "9. Digital filter".)

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

• Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) :
C1F2 (DA02) : Error correction status monitor output at C1 decode.
C2F1 (DA03) :
C2F2 (DA04) : Error correction status monitor output at C2 decode.
C2FL (DA05) : Correction status output, C2FL = C2F1·C2F2.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C210}}$ (DA14) : Bit clock (invert signal of $\overline{\text{C210}}$).
C210 (DA15) : Internal system clock (4.2336 MHz when DF is ON, 2.1168 MHz when CXD1125Q or DF is OFF).
DATA (DA16) : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

• Selection of offset binary/2's complement

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

• Selection of CD ROM/audio compatibility

When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

● Digital filter

The built-in digital filter has the following features:

1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

● Digital audio (D/A) interface

The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

● Countermeasures to defect

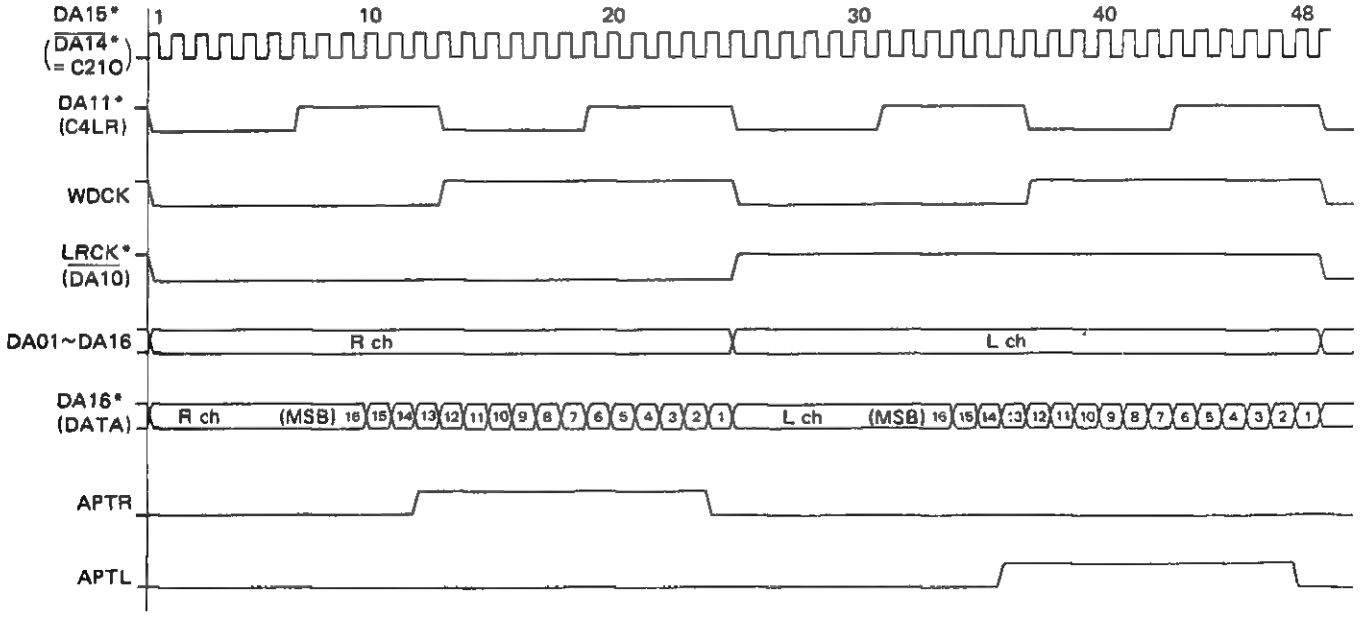
To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK Pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin.

However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

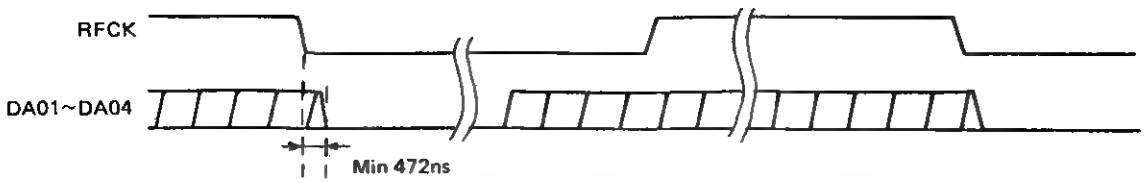
• Timing chart



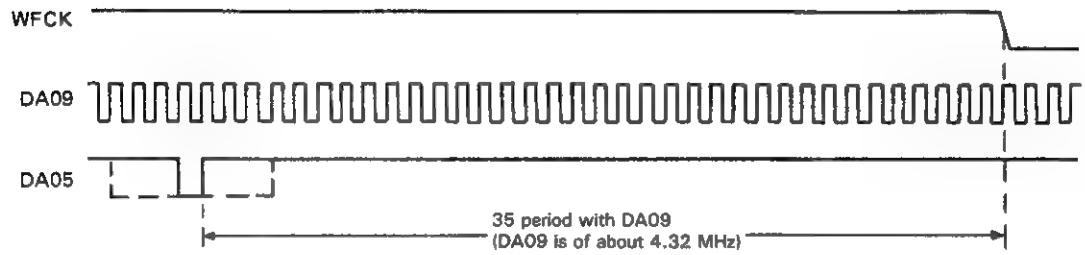
* When PSSL = "L".

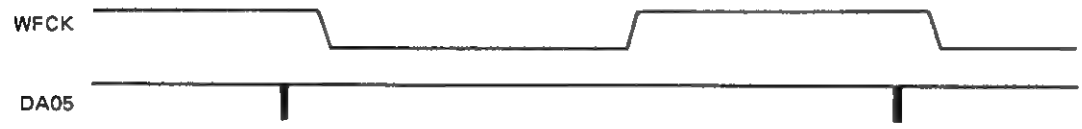
Fig. 7–15 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.





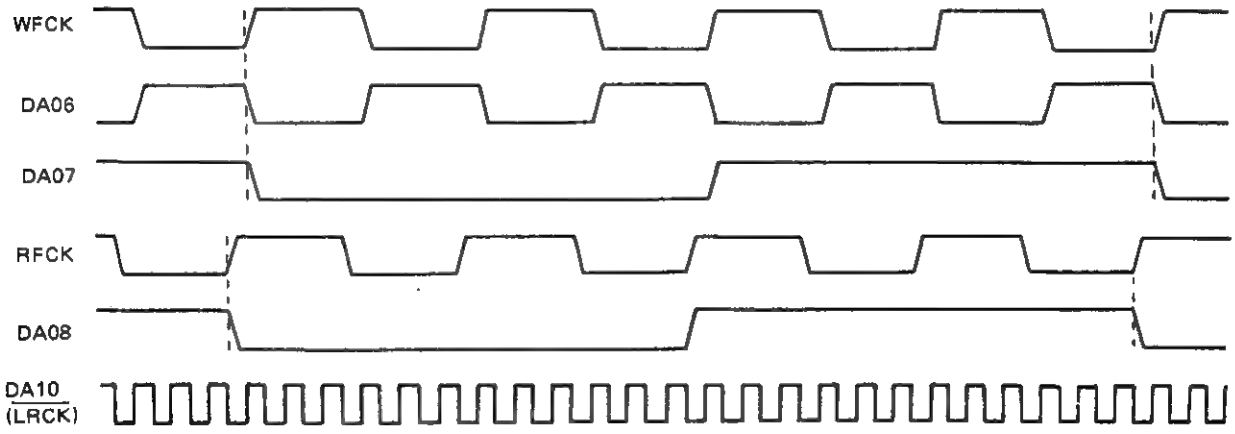


Fig. 7–16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

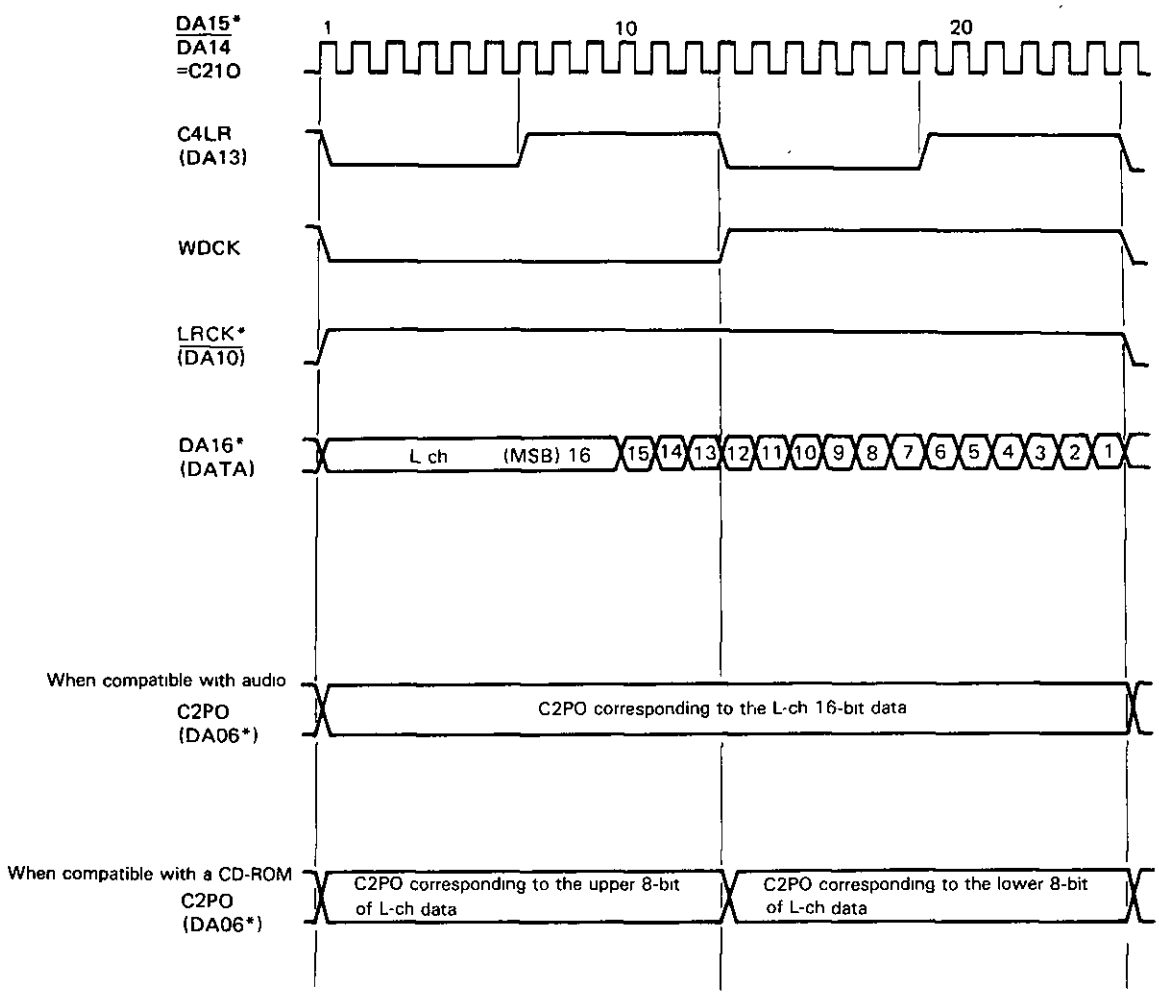


Fig. 7–17 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

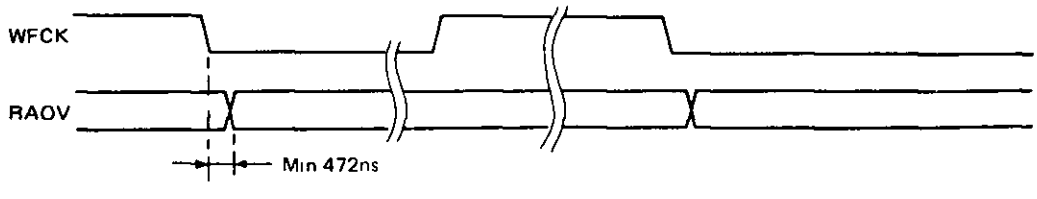


Fig. 7–18 Timing chart of RA0V output

CIRCUIT DESCRIPTION

8. D/A Converter TD6720N (X25-331X-XX : IC9)

TD6720N is a 16-bit Hi-Fi D/A converter of dual slope single integration type developed for PCM digital audio devices.

- This converter can be applied to 2's compliment code.
- This converter has a sampling holding circuit in it, thus the number of parts to be installed outside can be reduced.
- Sampling frequency of 30kHz to 100kHz can be applied to this converter. (This can be used as a double over-sampling D/A converter for CD player and DAT.)
- This converter has crystal oscillator amplifier in it.
- This converter outputs clock SCK of 1/4 frequency of f crystal.
- This converter performs D/A conversion of the signals of right and left channels alternately.

8–1. Terminal connection diagram

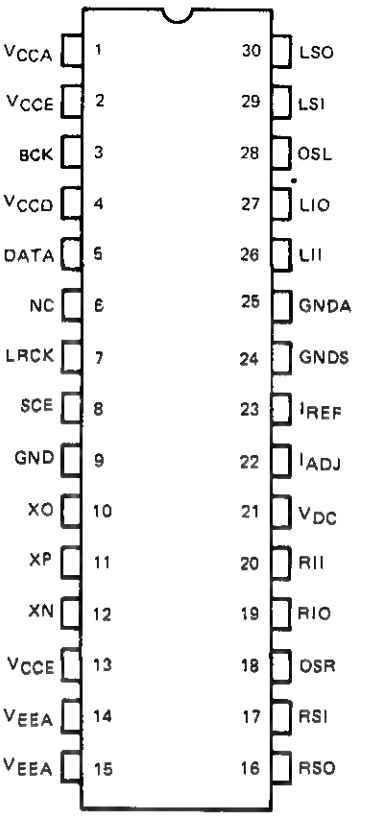


Fig. 8–1

8–2. Block diagram

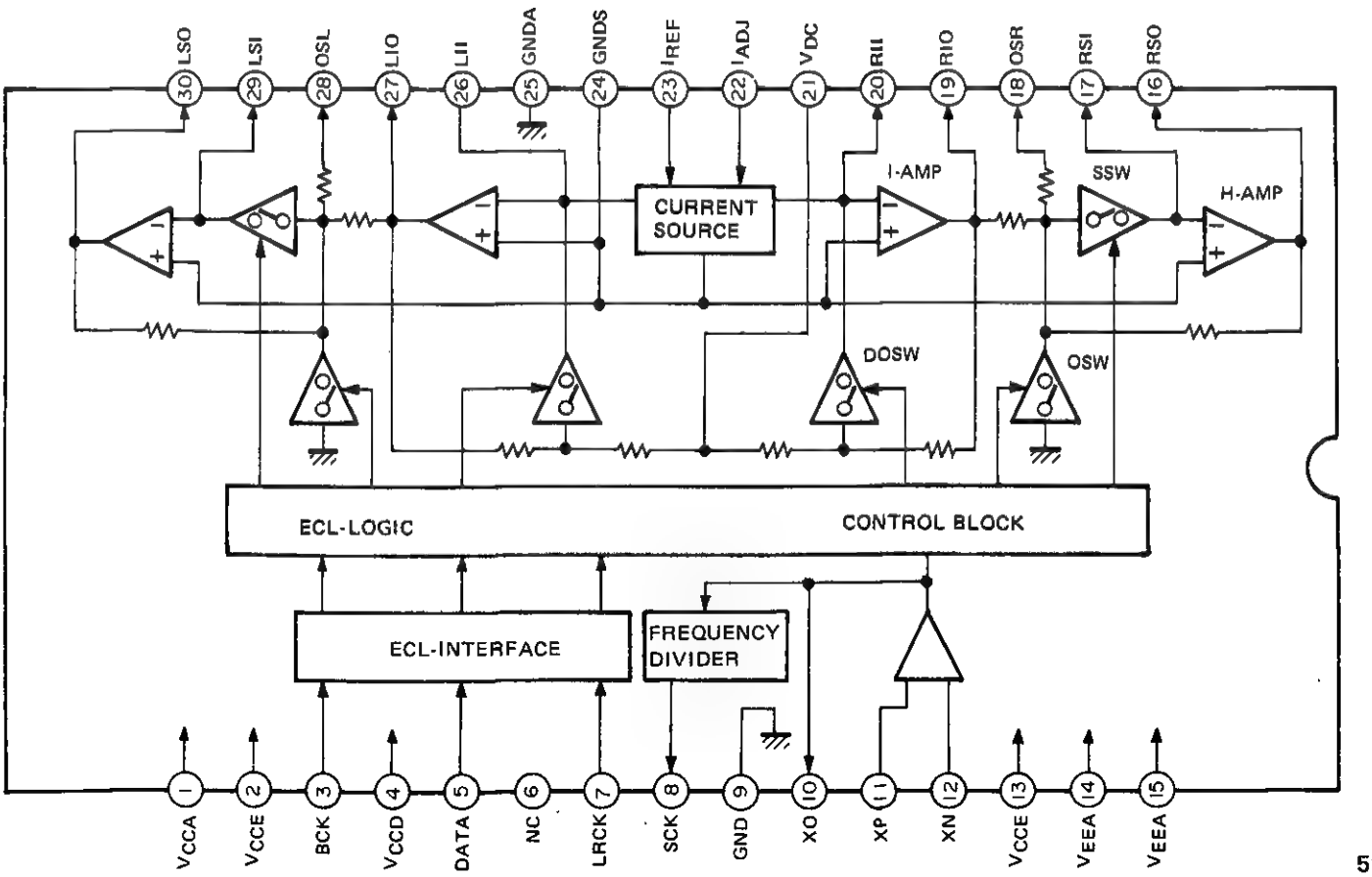


Fig. 8–2

CIRCUIT DESCRIPTION

8–3. Explanation of terminals

Terminal No.	Terminal name	Function
1	VCCA	Positive power supply voltage terminal for analog section (+5V).
2	VCCE	Power supply voltage terminal for ECL logic (+5V).
3	BCK	Bit clock input terminal. Duty cycle : 50%, f : 1.4112MHz.
4	VCCD	Power supply voltage terminal for digital section (+5V).
5	DATA	PCM digital audio data input terminal. Bit serial data (by unit of 16 bits) is input from MSB side synchronized with falling edge of BCK.
6	NC	Not connected.
7	LRCK	Input terminal of indicating signals of L ch and R ch of input data. Data must be input synchronized with falling edge of BCK.
8	SCK	System clock output terminal. Clock signal of 1/4 frequency of output of crystal oscillator is output. Can be used as system clock of signal processing system. When crystal frequency is 67.7376MHz, SCK is 16.9344MHz.
9	GND	ECL ground terminal.
10	XO	Input/output terminal for oscillating circuit. Modified Colpitts circuit is composed of SAW resonator or crystal oscillator,L, C and R.
11	XP	
12	XN	
13	VCCE	Power supply voltage terminal for ECL logic (+5V).
14, 15	VEEA	Negative power supply voltage terminal for analog section (−5V).
16	RSO	R ch sampling holding amplifier output terminal.
17	RSI	R ch sampling holding amplifier nagative input terminal.
18	OSR	R ch output offset adjustment terminal. Connected to GND A normally.
19	RIO	R ch integration amplifier output terminal.
20	RII	R ch integration amplifier negative input terminal.
21	VDC	Reference voltage terminal of discharge circuit.
22	IADJ	Current supply fine adjustment terminal. Connected to GND A normally.
23	IREF	Reference current input terminal. Recommended value : 0.5mA.
24	GND S	Ground terminal.
25	GND A	Analog ground terminal.
26	LII	L ch integration amplifier negative input terminal.
27	LIO	L ch integration amplifier output terminal.
28	OSL	L ch output offset adjustment terminal. Connectd to GND A normally.
29	LSI	L ch sampling holding amplifier negative input terminal.
30	LSO	L ch sampling holding amplifier output terminal.

Table 8–1

8–4. Explanation of function

- **Integration circuit and sampling holding circuit**

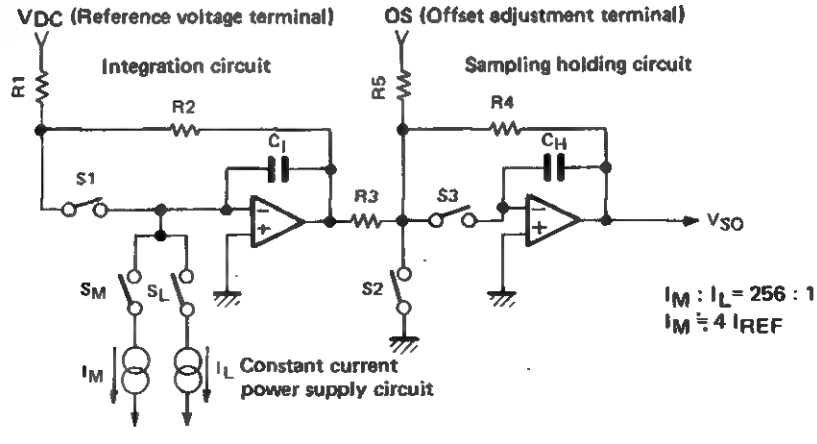


Fig. 8–3 Basic composition of integration circuit and sampling holding circuit

CIRCUIT DESCRIPTION

● **Basic operation of D/A conversion**

Step	S1	S2	S3	SM	SL	Contents of operation
1	OFF	ON	OFF	ON/OFF	ON/OFF	(Charging) Integrating operation – (Count– voltage) conversion S1 is turned off, and C_I is charged by two constant current supplies I_M and I_L. → D/A conversion of 16-bit digital data.
2		OFF	ON	OFF	OFF	(Sampling) S1 is turned off and S3 is turned on to take power accumulated in C_I into C_H.
3			OFF			(Holding) Charging potential of C_H just before turning off S3 (turning on S2) is held
4	ON	ON				(Discharge) Resetting operation S1 is turned on and C_I is discharged until reference voltage V_{RS} is obtained. $V_{RS} = -\frac{R2}{R1} \times V_{DC} = -\frac{4\,k\Omega}{6\,k\Omega} \times 5 = -3.3V$

Table 8–2

● **Timing chart**

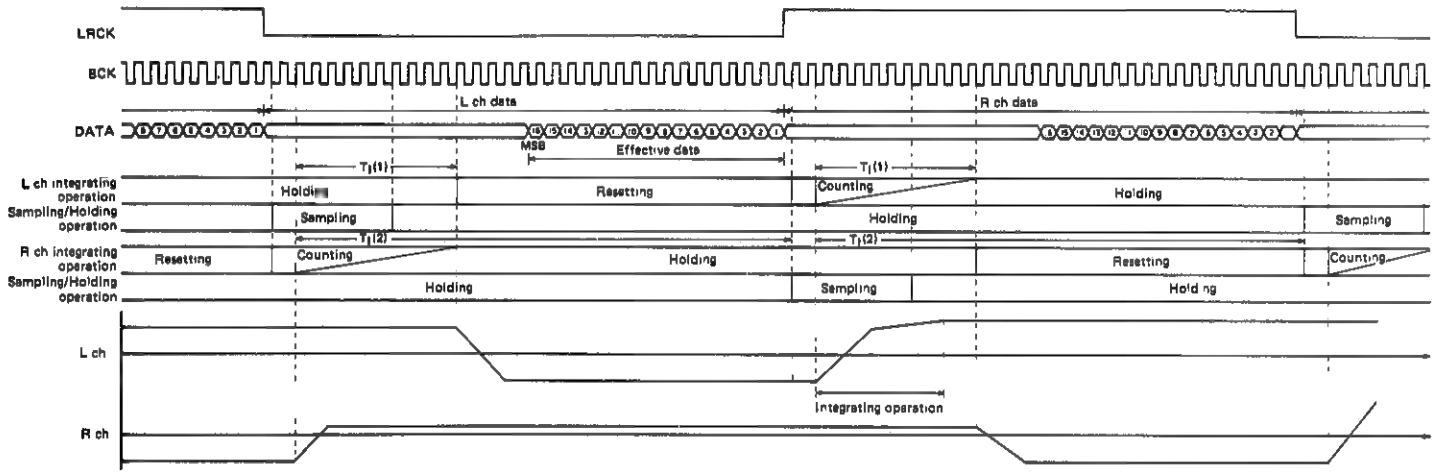
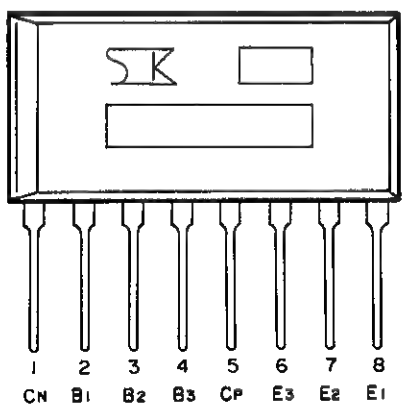


Fig. 8–4 Timing chart in case $f_{BCK} = 64f_{LR}$

9. Driver STA341M (X25-331X-XX : Q25)

9–1. Terminal connection diagram



E : Emitter
B : Base
C : Collector

Fig. 9–1

9–2. Equivalent circuit

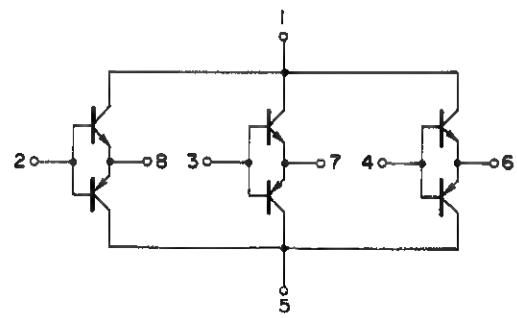


Fig. 9–2

MECHANISM OPERATION DESCRIPTION

Mechanism operation description

Fig. 1 snows the mechanism positioning in the STOP mode. The OPEN/CLOSE operation when loading the disc is described below.

Note :

In the operation description, the black and white arrows shows the following code :

Black arrow : Shows the opening direction of the tray (Tray OPEN).

White arrow : Shows the closing direction of the tray (Tray CLOSE).

Also in the operation description and illustrations, numbers in brackets ( ) followed by the part name show the identifying numbers of the disassembly diagram in the Service Manual.

1. OPEN/CLOSE operation

The center of the OPEN/CLOSE lug detection leaf switch installed on the PC board (J25-5506-02(A/3)) on the rear of the mechanism is pressed to the right by lower side of the tip of the black switch arm (6) installed on the slider ass'y (11) when the tray is closed, and the information is transferred to the microprocessor. This status is called the tray CLOSE operation. The operation from this status to the condition when the tray is completely opened by pressing the OPEN/CLOSE key is described.

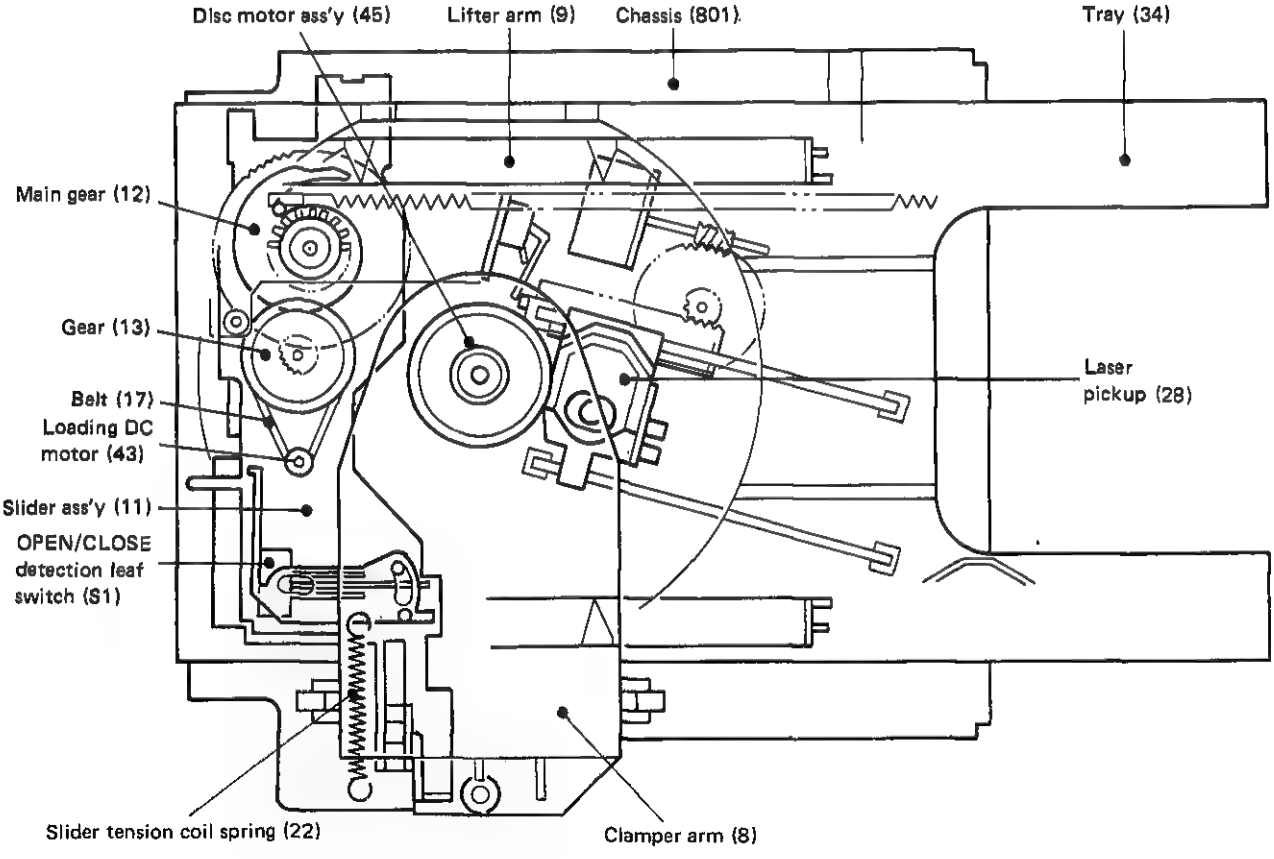


Fig. 1 Tray closed status

MECHANISM OPERATION DESCRIPTION

As shown in Fig. 2, loading DC motor (43) rotates in the direction of the black arrow ❶ and transfers the rotation of the black arrow ❷ to the gear (13) via the belt (17), and also rotates the main gear (12) in the direction of the black arrow ❸ with the lower gear section of the gear (13). The main gear (12) contains the cam on its upper surface. Along with the surface of the cam, protrusion A located in the lower side of the slider ass'y (11) is shifted and the slider ass'y (11) begins to move in the direction of the black arrow ❹.

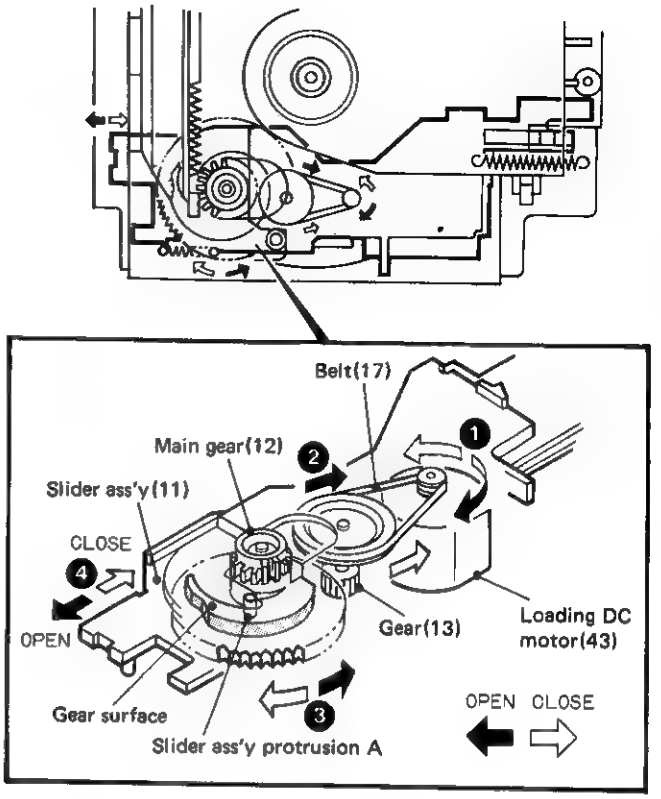


Fig. 2 Loading motor rotation transmission

Fig. 3 shows the movement of protrusion A of the slider ass'y(11) in the direction of the black arrow ❹ until the tray is completely opened.

The slider ass'y(11) releases the OPEN/CLOSE detection leaf switch(S1) from the CLOSE condition and pulls the foot section of the clamper arm(8) in the direction of the black arrow ❹ by the groove section of the slider ass'y(11). By this, the clamper arm(8) is lifted in the direction of the black arrow ❻ with a support as a center to the disc release condition from the disc clamping condition.

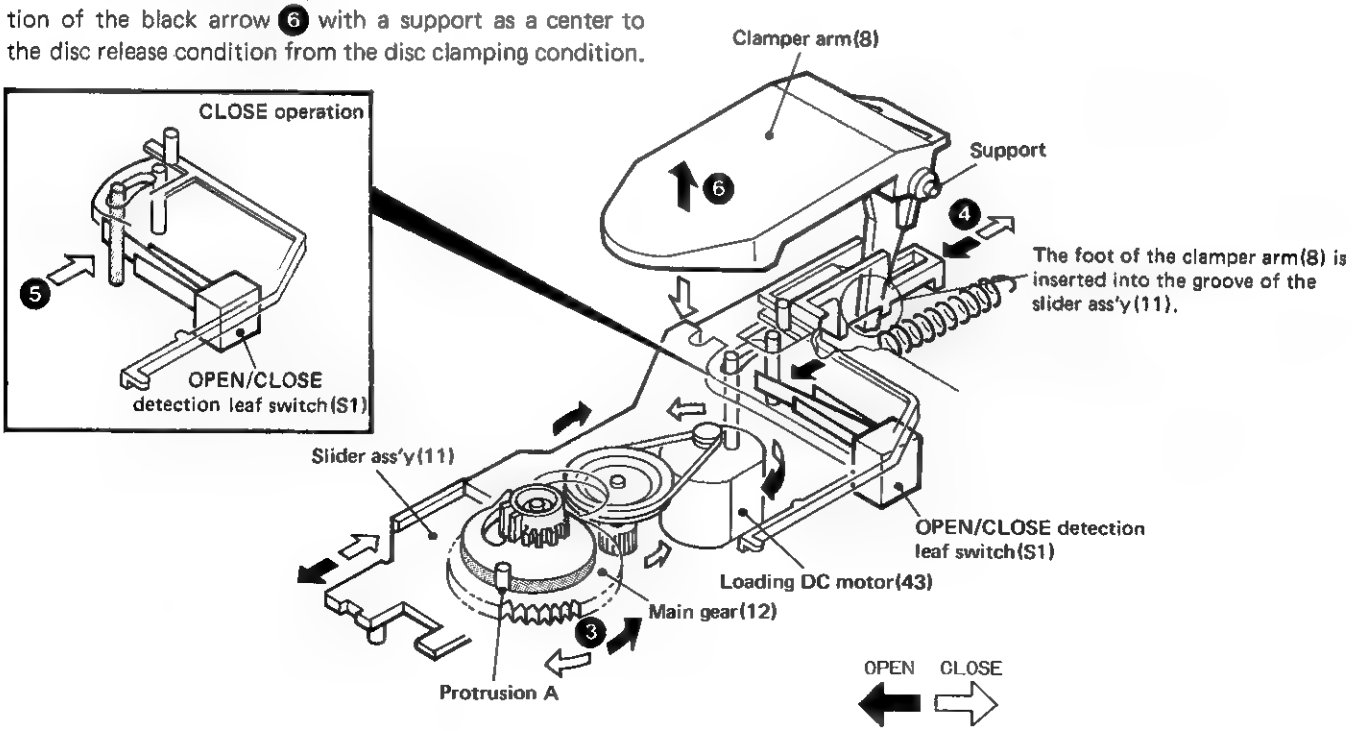


Fig. 3 Clamper arm operation

MECHANISM OPERATION DESCRIPTION

Fig. 4 shows the condition when the tray is completely opened. The tray is "sloped" as shown in the figure. When the tray moves in the direction of the black arrow ❺ OPEN direction, the white protrusion climbs the "slope" to short the OPEN/CLOSE detection leaf switch(S1) in the reverse direction of the STOP condition, then informs the microprocessor that the OPEN operation has completed and to stop the rotation of the loading DC motor(43).

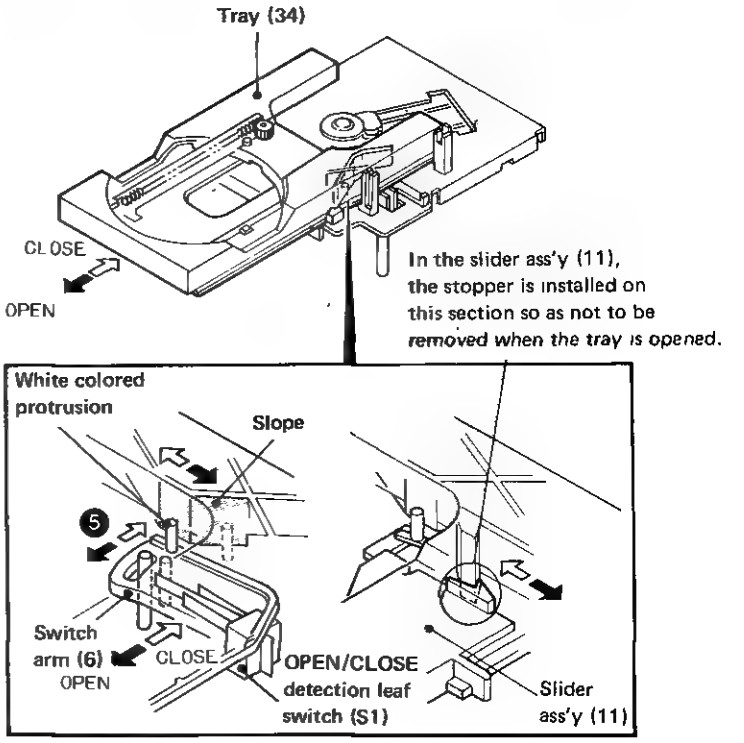


Fig. 4 Each limit switch when opening/closing the tray

Fig. 5 shows the OPEN operation until the disc is lifted from the turntable and placed on the disc tray so that the disc is removed from the player. These operations are performed almost at the same time as the up operations of the clamper arm(8) when the tray is opened as described in Fig. 2 to 4 above.

The tray(34) incorporates the lifter arm(9) which is required to support the disc when the tray is opened/closed and the lifter slider(10) which drives the lifter.

When the tray is opened, the slider ass'y(11) is shifted in the direction of the black arrow ❹. In the slider ass'y, lug a is installed to slide the lifter slider horizontally (toward the left and right). And the lifter slider(10) is always pulled in the direction of the black arrow ❼ by the tray ass'y tension coil spring(25).

For this, when the slider ass'y(11) is moved to the OPEN direction (in the direction of the black arrow ❹), the lifter slider(10) is also shifted to the left by the lug a. The lifter slider(10) has grooves on its left and right ends to lift the lifter arm up/down.

In the OPEN operation, when the lifter slider(10) is moved in the direction of the black arrow ❼, protrusion B of the lifter arm(9) is slide in the groove using the support as a center, and the lifter arm is lifted in the direction of the black arrow ❽.

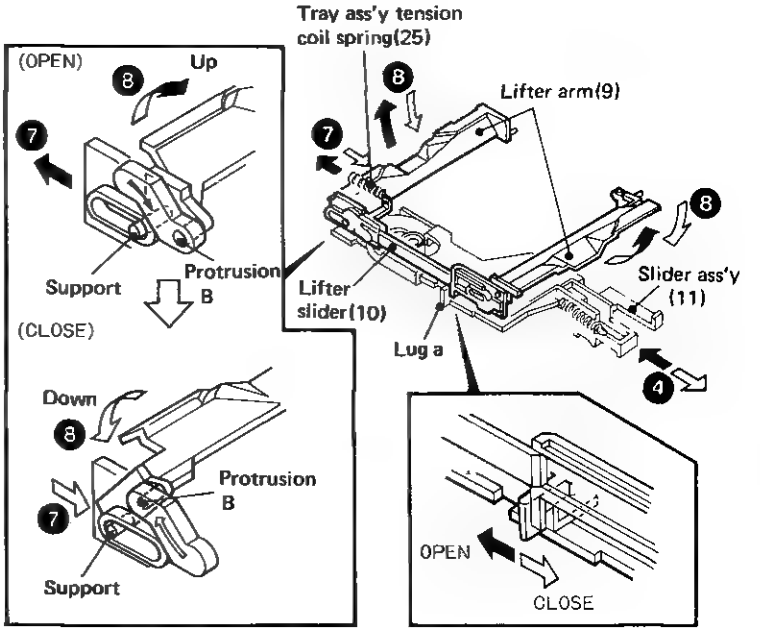


Fig. 5 Lifter arm up/down operation

MECHANISM OPERATION DESCRIPTION

Fig. 6 shows the operation of the main gear(12) which actually performs the OPEN/CLOSE operation of the tray described above.

In the upper surface of the main gear(12), there's a gear to open or close the tray. Among the gear teeth, only two teeth are longer than the other, for triggering the OPEN operation.

First these longer teeth trigger the OPEN operation, then the whole gear engages the gear rack of the surface of the tray to initiate the OPEN operation.

At this time, protrusion A installed on the lower side of the slider ass'y(11) is located at the position where the main gear(12) is rotated approx. 360 degree from the STOP position. At this position, when the triggering gear and the gear rack of the tray are engaged to initiate the OPEN operation, protrusion A will drop to the STOP position again from the convex of the main gear(12) cam surface. To prevent this, the white colored roller installed on the slider ass'y(11) releases protrusion A from the cam surface of the main gear(12), so as not to contact with the cam surface while the main gear(12) is engaged with the gear rack on the back of the tray in OPEN/CLOSE operation.

Since this roller is always pulled in the right direction (viewd from the front) by the slider tension coil spring(22) and the arm pressure coil spring(24), it slides while pressing the guide surface on the back of the tray in the right direction in the tray OPEN/CLOSE operation.

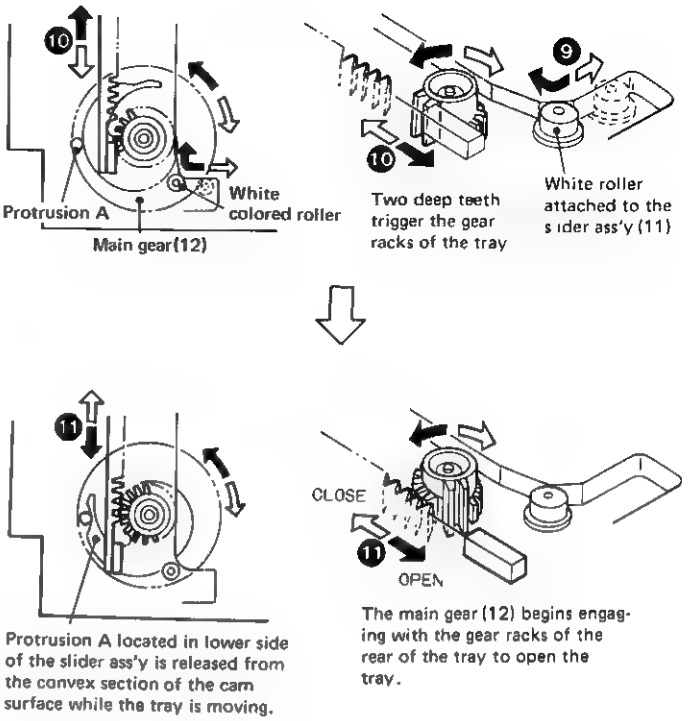


Fig. 6 Gear (12) operations

2. Disassembling procedure of mechanism section

2–1. Removing the clamper arm

1) While lightly pressing the clamper arm from the top ❶ , remove the fixing lugs on both sides in the direction of arrows ❷ and ❸ .
2) Remove the clamper arm in the direction of arrow ❹ .

Note : Be sure to remove the fixing lugs on both sides of the clamper arm while pressing the clamper arm in the direction of arrow ❶. Since the lugs are solid, if forcibly performed, they might be broken.

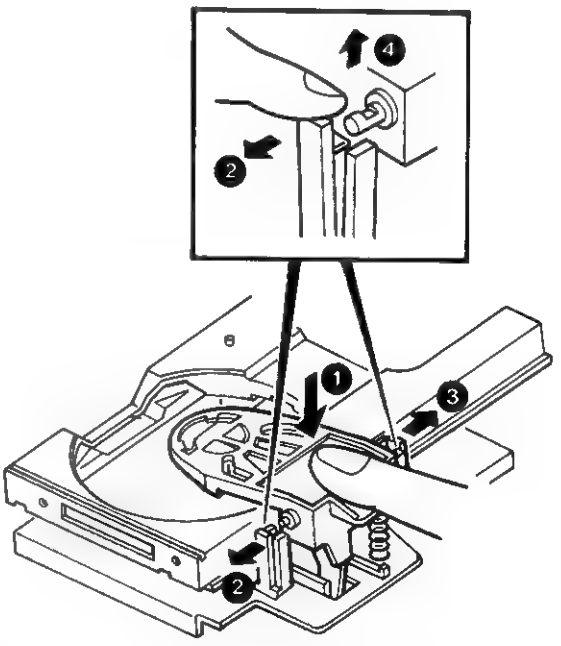


Fig. 1 Removing the clamper arm

MECHANISM OPERATION DESCRIPTION

2–2. Attaching the clamper arm

1) Insert the foot section of the clamper arm into the groove of the slider ass'y (❺).
2) At this time confrim that portrusion A of the clamper arm is inserted into the center of the arm pressure coil spring.
3) Put the support of the clamper arm to the lug section of the outsert of the mechanism by pressing from the top (❻).

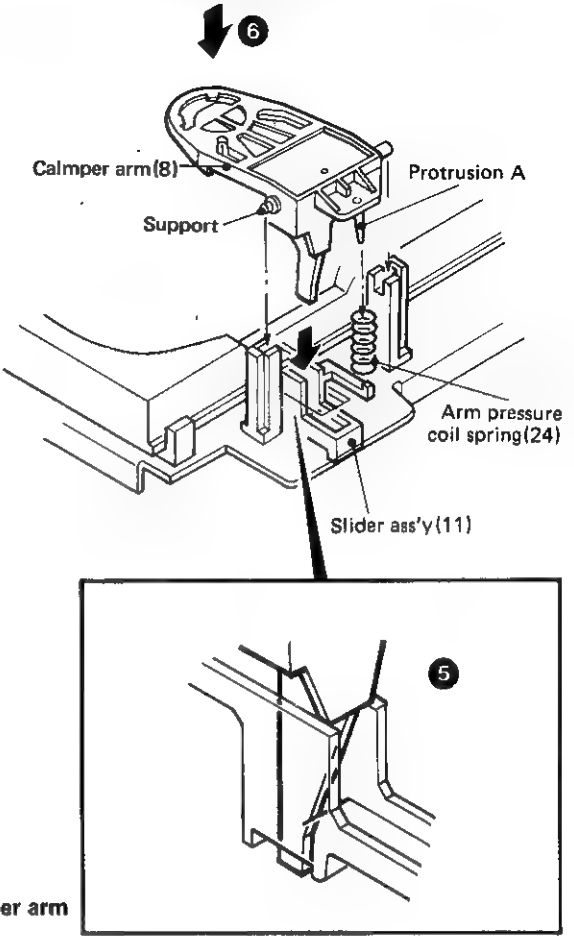


Fig. 2 Attaching the clamper arm

2–3. Removing the tray

1) While pressing the hook section of the slider ass'y in the direction of arrow ❼ , pull out the tray in the direction of arrow ❽ to remove it (❾).

Note : Be sure not to release your finger when pressing the hook. If the hook is released, the stopper on the upper surface of the slider ass'y will come in contact with the stopper of the tray and the tray will not be removed.

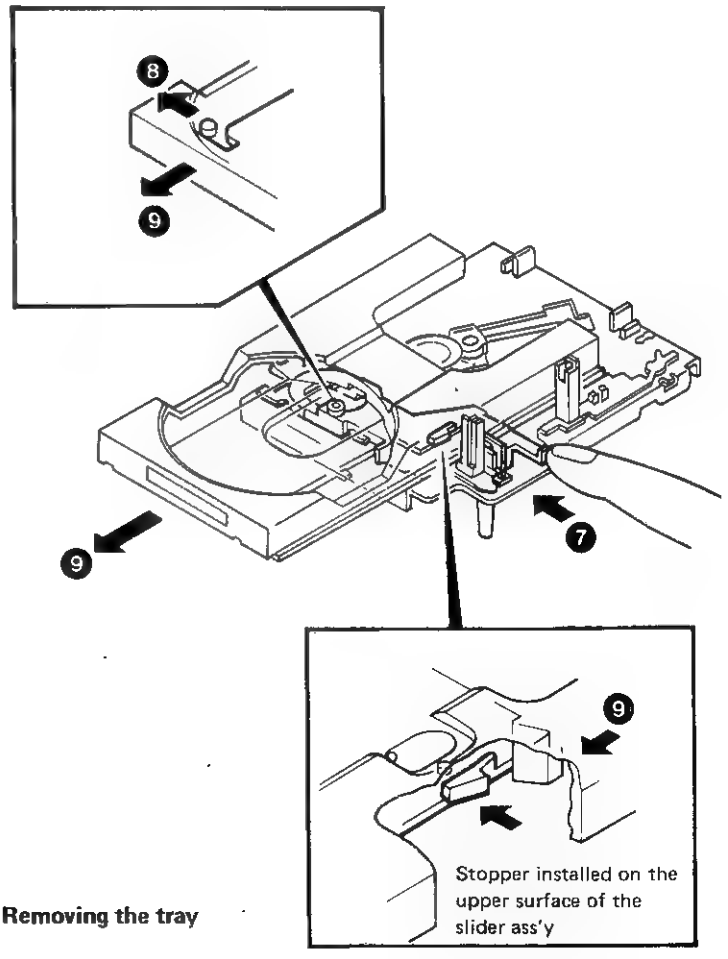


Fig. 3 Removing the tray

MECHANISM OPERATION DESCRIPTION

2–4. Attaching the tray

1) Attach the collars firmly on both sides of the tray to the four section supporting and guiding the tray as shown in the Fig. 4.
   First attach the front two section then attach the rear two sections as shown in ⑩.

Note : The gear offset of the mechanism after removing/ attaching the tray will be reset automatically by performing the OPEN/CLOSE operation

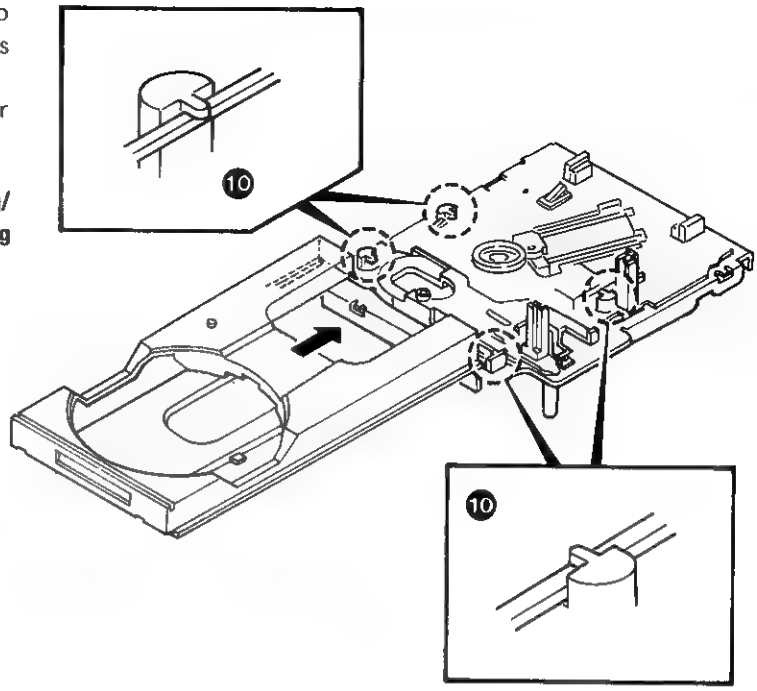


Fig. 4 Attaching the tray

2–5. Removing the slider ass'y

1) Removing the slider tension coil spring attached to the slider ass'y (⑪).
2) Slide the slider ass'y in the direction of arrow ⑫ until it reaches the position where it can be removed from the outsert section supporting the slider ass'y.
3) Remove the slider ass'y by pulling out right above in the direction of arrow ⑬ .

Note : If the slider ass'y is removed askew, the OPEN/ CLOSE detection leaf switch on the back of the tray might be bent down.

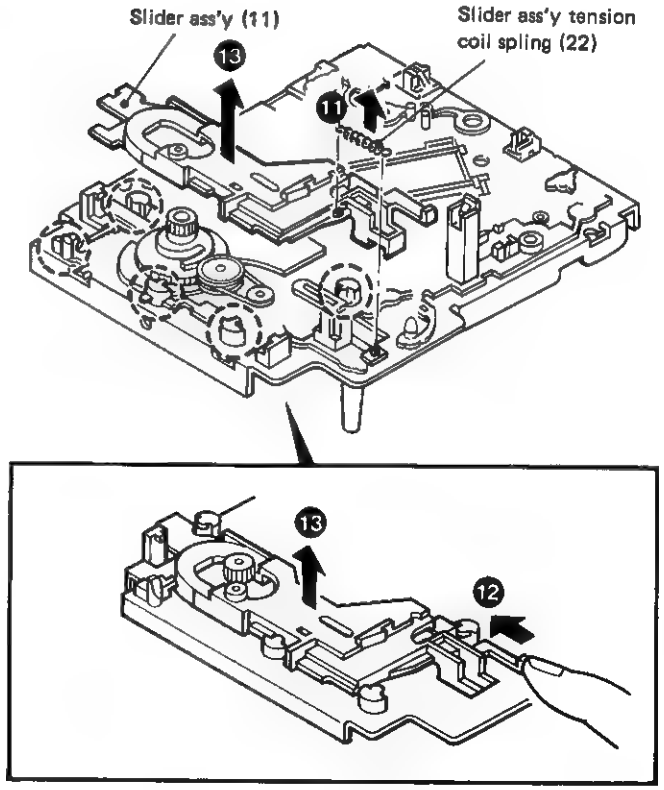


Fig. 5 Removing the slider ass'y

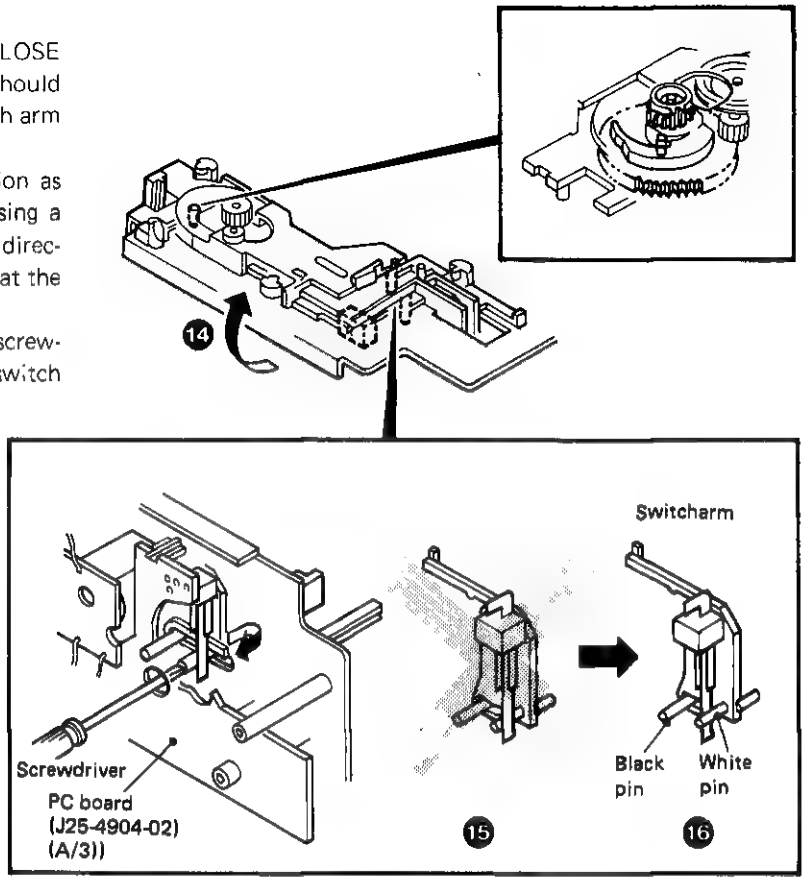
MECHANISM OPERATION DESCRIPTION

2–6. Attaching the slider ass'y

The long metal piece at the center of the OPEN/CLOSE detection leaf switch on the rear of the mechanism should be set between the white and black pins of the switch arm installed on the rear of the slider ass'y.

If it is inserted simply, it will be set the position as shown in ⑮. At this time, correct the position using a screwdriver by lifting the slider ass'y slightly in the direction ⑭ so that the white pin of the switch arm is set at the position as shown in ⑯.

A round hole is on the PC board for inserting the screwdriver. This is used for correcting/checking the switch position when working.



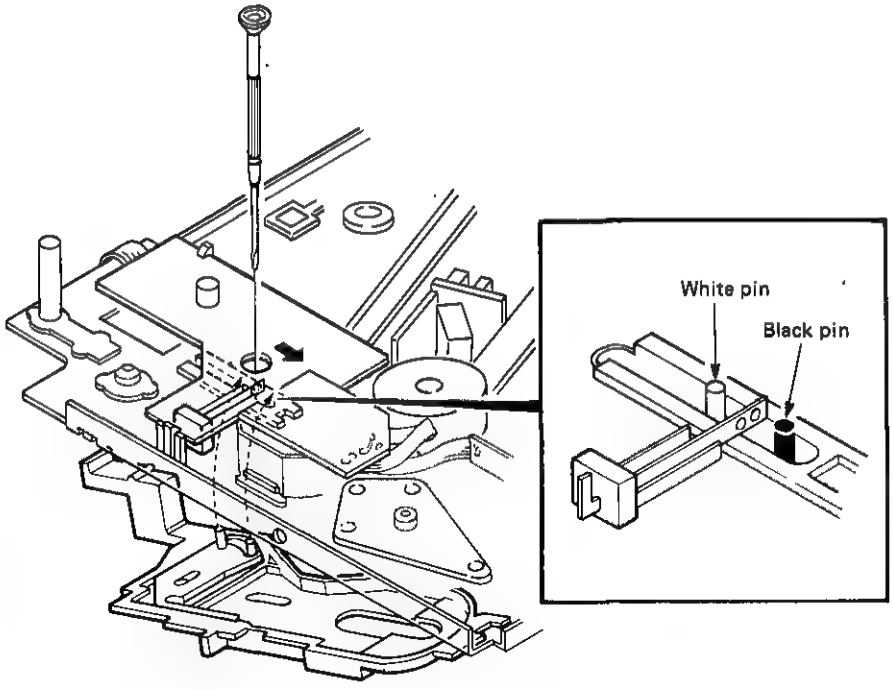


Fig. 6 Attaching the slider ass'y

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	–	Apply the sensor section of the optical power meter on the pickup lens.	Short circuit pins TEST and turn power on to enter the Test mode. Press the SEARCH key to move the picup to the outermost position. Press the CHECK key, the LD should emit light. Check that the display is "03".	–	When the power is from 0.2 to 0.3mW, RF level is 2.0Vp-p or more, TE(servo open) is 1.5Vp-p or more and the diffraction grating is aligned correctly, the pickup is acceptable.	(a)
2	VCO	–	Connect a frequency counter to pin 9(PLCK) (X25-331)	Press the STOP key, and confirm that the display is "01".	L5 (X25-331)	4.30MHz	(b)
3	TRACKING ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1890 pin 1) CH2: TE (X25-331 pin 1)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK key and confirm that the display is "03".	TE.BALANCE VR2 (X29-1890)	Symmetry between upper and lower patterns, or DC=0±0.05V	(c)
4	FOCUS ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1890 pin 1) CH2: TE (X25-331 pin 1)	PLAY	FE BALANCE VR1 (X29-1890)	Optimum eye pattern	(d)
5	FOCUS GAIN	Test disc Type 4 Apply 1kHz, 0.5Vrms signal to CN5 pin 2 of PC board (X25-331)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 1 of CN5 via a 47kΩ, 470 pF LPF.(X25-331)	PLAY	FOCUS GAIN VR1 (X25-331)	50mVrms	(e)
6	TRACKING GAIN	Test disc Type 4 Apply 1kHz, 0.5Vrms signal to CN5 pin 4 of PC board (X25-331)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 5 of CN5 via a 47kΩ, 470 pF LPF.(X25-331)	PLAY	TRACKING GAIN VR2 (X25-331)	50mVrms	(e)

(Note) Type 4 disk: SONY YEDS-18 Test Disk or equivalent.

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre l'alimentation en circuit pour entrer en mode de test. Presser la touche SEARCH pour déplacer le capteur jusqu'à la position la plus externe. Presser la touche CHECK, la diode devrait émettre de la lumière. Vérifier que l'affichage est " 03 ".		Quand l'alimentation est de 0,2 à 0,3mW, le niveau RF de 2,0Vc-c ou plus, TE (asservissement ouvert) de 1,5Vc-c ou plus et le réseau de diffraction aligné correctement, le capteur est acceptable.	(a)
2	VCO	–	Raccorder un compteur de fréquence à broche 9 (PLCK). (X25-331)	Presser la touche STOP et s'assurer que l'affichage est " 01 ".	L5 (X25-331)	4,30MHz	(b)
3	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1890 broche 1) CH2: TE (X25-331 broche 1)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est " 03 ".	TE BALANCE VR2 (X29-1890)	Symétrie entre les formes supérieure et inférieure ou DC=0±0,05V	(c)
4	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1890 broche 1) CH2: TE (X25-331 broche 1)	PLAY	FE BALANCE VR1 (X29-1890)	Forme optimum	(d)
5	GAIN DE MISE AU POINT	Disque test Type 4 Appliguer un signal 1kHz, 0,5Vrms à la troche 2 de CN5 sur la plaquette X25-331.	Utiliser un gabarit d'asservissement ou raccorder un oscilloscope ou un voltmètre CC à la broche 1 de CN5 via un FPB de 47kΩ, 470 pF.	PLAY	GAIN DE MISE AU POINT VR1 (X25-331)	50mVrms	(e)
6	GAIN D'ALIGNMENT	Disque test Type 4 Appliguer un signal 1kHz, 0,5Vrms à la troche 4 de CN5 sur la plaquette X25-331.	Utiliser un gabarit d'asservisement ou raccorder un oscilloscope ou un voltmètre CC à la broche 5 de CN5 via un FPB de 47kΩ, 470 pF.	PLAY	GAIN D'ALIGNEMENT VR2 (X25-331)	50mVrms	(e)

(Remarque)Disque de type 4:Disque test SONY YEDS-18 ou équivalent.

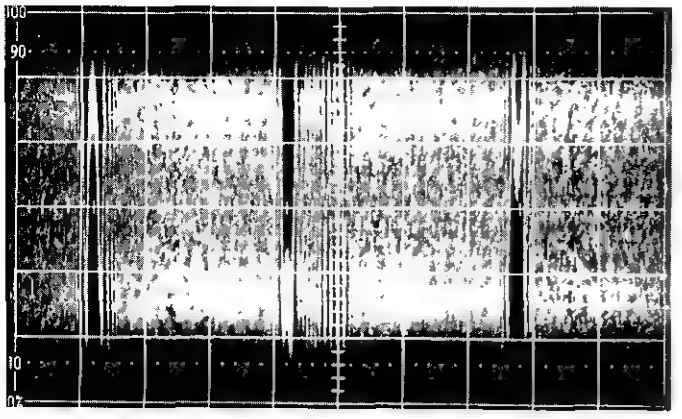
ABGLEICH

NR.	GEGENSTAND	EINGANGS EINSTELLUN	AUSGANGS EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test Modus zu aktivieren. Die Taste SEARCH drücken, um den Abnehmer ganz nach außen zu bringen. Die Taste CHECK drücken, dann muß die LD Licht abstrahlen. Prüfen, daß " 03 " angezeigt wird.	–	Wenn bei einer Spannung von 0,2 bis 0,3 mW der RF-Pegel 2,0Vs-s oder mehr, TE (Servo-Offen) 1,5Vs-s betragt und das Beugungsgitter richtig ausgerichtet ist, ist der Abtaster in Ordnung.	(a)
2	VCO	–	Einen Frequenzzähler an Stift 9(PLCK) anschließen. (X25-331)	Die STOP-Taste drücken und prüfen, daß " 01 " auf dem Display angezeigt wird.	L5 (X25-331)	4,30MHz	(b)
3	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1890 Stift 1) Kanal 2: TE (X25-331 Stift 1)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß " 03 " auf dem Display angezeigt wird.	TE BALANCE VR2 (X29-1890)	Symmetrie zwischen oberen und umteren Mustern oder Gleichstrom DC=0±0,05V	(c)
4	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oazilloskop wie folgt anschließen: Kanal 1: RF (X29-1890 Stift 1) Kanal 2: TE (X25-331 Stift 1)	PLAY	FOKUS-FEHLERAUSGLEICH VR1 (X29-1890)	Optimales Augenmuster	(d)
5	FOKUSVERSTÄRKUNG	Testdisc Typ 4 Ein 1kHz, 0,5Vrms Signal an Stift 2 von CN5 an platine X25-331 anlegen.	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 1 von CN5 über ein 47kΩ, 470pF Tiefpaßfilter anschließen.	PLAY	FOKUSVERSTÄRKUNG VR1 (X25-331)	50mVrms	(e)
6	SPURHALTE-VERSTÄRKUNG	Testdisc Typ 4 Ein 1kHz, 0,5Vrms Signal an Stift 4 von CN5 an platine X25-331 anlegen.	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 5 von CN5 über ein 47kΩ, 470pF Tiefpaßfilter anschließen.	PLAY	SPURHALTE-VERSTÄRKUNG VR2 (X25-331)	50mVrms	(e)

(Hinweis) Typ 4 Disc: SONY YEDS-18 Testdisc oder Äquivalent.

ADJUSTMENT/REGLAGE/ABGLEICH

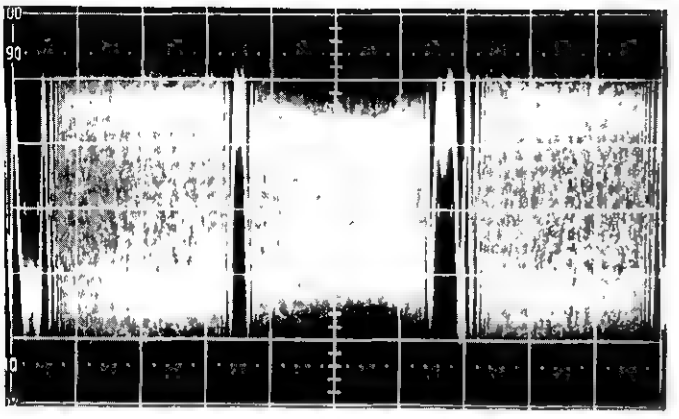
DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG



Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

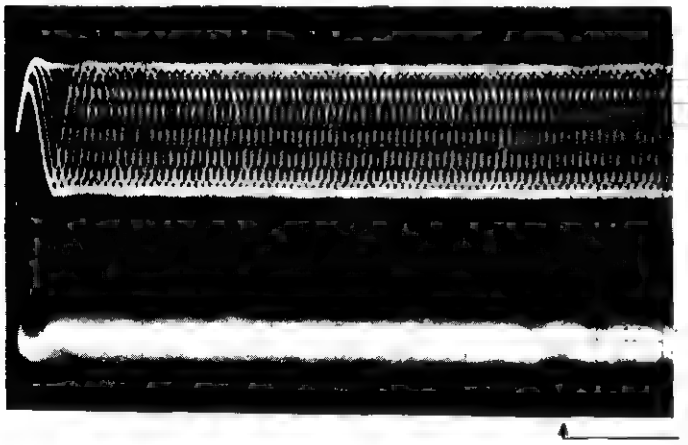
Tracking error waveform
Upper : 0.5V/div.
Lower : 20ms/div
Forme d'onde d'erreur d'alignement
Supérieure : 0.5V/div.
Inférieure : 20ms/div.
Spurhaltefehler-Wellenform
Oben : 0.5V/Teilung
Unten : 20ms/Teilung

Photo 1
Photo 1
Foto 1



Incorrect (shifted) waveforms
Forme d'onde incorrecte (dérivée)
Falsche (verschobene) Wellenform

Photo 2
Photo 2
Foto 2

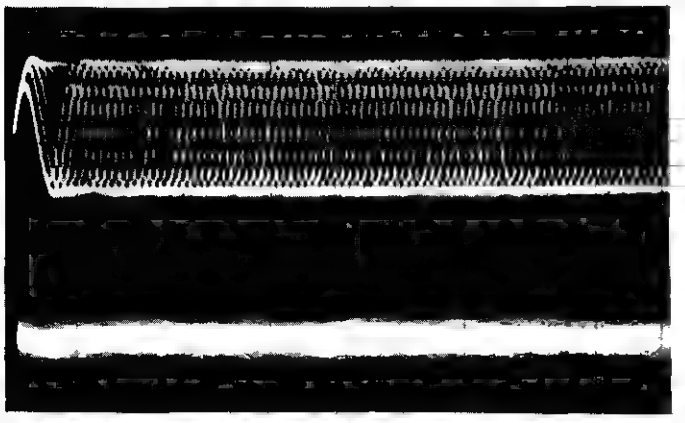


Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

Upper : RF signal 1V/div.
Lower : Sub spot beam signal 0.1V/div.
0.5μs/div.
Supérieure : signal HF 1V/div.
Inférieure : signal de rayon spot auxiliaire 0.1V/div.,
0.5μs/div.
Oben : HF-Signal 1V/Teilung
Unten : Nebenpunktstrahl-Signal 0,1V/Teilungs,
0,5μs/Teilung

Photo 3
Photo 3
Foto 3

17~18μs later
17~18μs us plus tard
17~18μs später

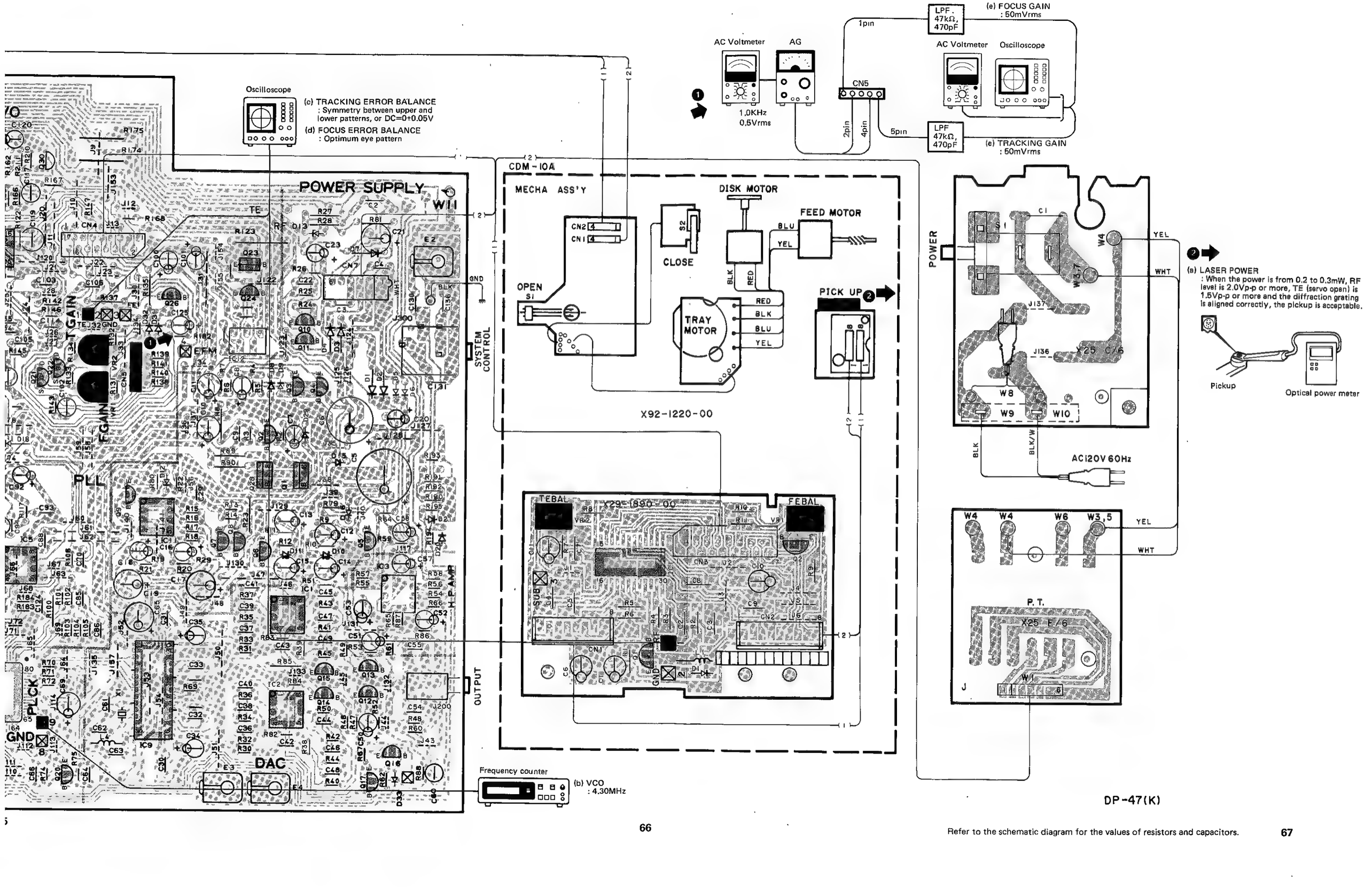


Waveform when the sub beam is shifted to the adjacent track.
Forme d'onde quand le rayon auxiliaire est décalé sur la piste adjacente.
Wellenform, wenn der Nebenstrahl zur benachbarten Spur verschoben ist.

Photo 4
Photo 4
Foto 4

FRONT
PICK UP
SERVO
SYSTEM CONTROL
J25-5814-01
X25-3310-11
TEST MODE
RMUTE
DGND
PLCK
EFM DEC
CN1
CN2
CN3
CN6
FL1
CMK-54X@VU
X25-3270-11
OP/CL
TIME
REP
FB
FF
DOWN
UP
P-MODE
STOP
PLAY
CHK
CLR

PC BOARD VIEW (COMPONENT SIDE VIEW)



DP-47(K)

Refer to the schematic diagram for the values of resistors and capacitors.

X25-331X-XX

	B	C	E
Q1	5.8V	8.4V	5.2V
Q2	0.6V	5.8V	0V
Q3, 4	5.6V	8.6V	−5.0V
Q5	6.7V	8.3V	6.1V
Q6	−6.8V	−8.6V	6.1V
Q7, 8	7.7V	5.1V	—
Q9	7.9V	5.1V	−8.6V
Q10	−30.6V	−32.5V	-30.0V
Q11	−5.5V	−30.6V	−5.0V
Q12, 13	0.7V	0V	0V
Q14, 15	−6.1V	0V	0V
Q16	5.5V	−6.1V	6.1V
Q17	−6.1V	3.4V	−6.1V
Q18	0.6V	8.4V	0V
Q19	0.6V	8.6V	0V
Q20	0.6V	2.1V	0V
Q23	0.7V	8.4V	0V
Q24	−0.7V	−8.6V	0V
Q26	4.5V	5.1V	5.1V
Q27	−7.3V	5.0V	0V
Q28	5.8V	8.4V	5.2V
Q29	0V	0.7V	0V
Q31	0V	4.2V	0V

	G	S	D
Q21, 22	0V	0V	0V

Q25

1	8.4V
2	0.5V
3	0.5V
4	-1.1V
5	−8.6V
6 – 8	0V

IC1, 2

1 3	0V
4	−6.1V
5 – 7	0V
8	6.1V

IC4

1	−7.4V
2	5.1V
3	4.2V
4	−8.7V
5, 6	0V
7	0.5V
8	8.5V

IC5

1	0V
2, 3	2.6V
4	−8.7V
5, 6	0V
7	0.6V
8	8.5V

IC6

1 – 5	0V
6 – 10	5.1V
11 13	0V
14	4.1V
15	5.1V
16	0.1V
17	−5.0V
18 - 20	0V
21	−0.7V
22	0V
23	−0.6V
24, 25	0V
26	5.1V
27	−0.6V
28 30	0V

IC7

1 3	0V
4	0.1V
5	4.3V
6	4.5V
8	0V
9	2.5V
10	0V
11	2.5V
12	0V
13 – 15	5.0V
16	4.9V
17	4.5V
18	0V
19	5.1V
20	0V
23, 24	0V
25	2.6V
26	0V
28	0V
29 32	0.6V
33	5.0V
34, 35	2.7V
36	2.2V
37	4.3V
38 44	2.4V
45	2.7V
46	2.3V
47	2.4V
48	2.8V
49	4.3V
50	2.0V
51	1.3V
52	0V
53	1.8V
55	0V
56	5.0V
57 59	0V

IC8

1 – 7	2.4V
8, 9	2.7V
10, 11	0.6V
12	0V
13, 14	0.6V
15	2.7V
16	2.2V
17	4.3V
18	2.0V
19	2.3V
20	2.0V
21	4.3V
22	2.8V
23	2.4V
24	5.0V

IC9

1, 2	5.1V
3	2.1V
4	5.1V
5	0V
7	2.6V
8	4.2V
9	0V
10	5.1V
11	3.0V
12	2.7V
13	5.1V
14, 15	−5.1V
16	−0.6V
17, 18	0V
19	−0.8V
20	0V
21	5.1V
22	0V
23	−3.7V
24 – 26	0V
27	0.8V
28, 29	0V
30	−0.6V

IC10

1 - 4	−11.7V
5	0V
6	2.6V
7, 8	0V
9	5.0V
10 13	0V
14 16	5.1V
18	0.6V
19	5.1V
20	0.6V
21 – 24	0V
25 – 28	5.1V
30	1.3V
32	0V
35 – 38	0V
39	5.0V
40 – 48	26.5V
54	22.7V
55	11.7V
56	30.0V
57	-5.0V
58	−22.7V
59	−15.6V
61	−15.7V
62, 63	−22.0V
64	5.2V

IC11

1	2.8V
2, 3	0V
4	8.6V
5, 6	3.0V
7	5.9V
8	8.4V

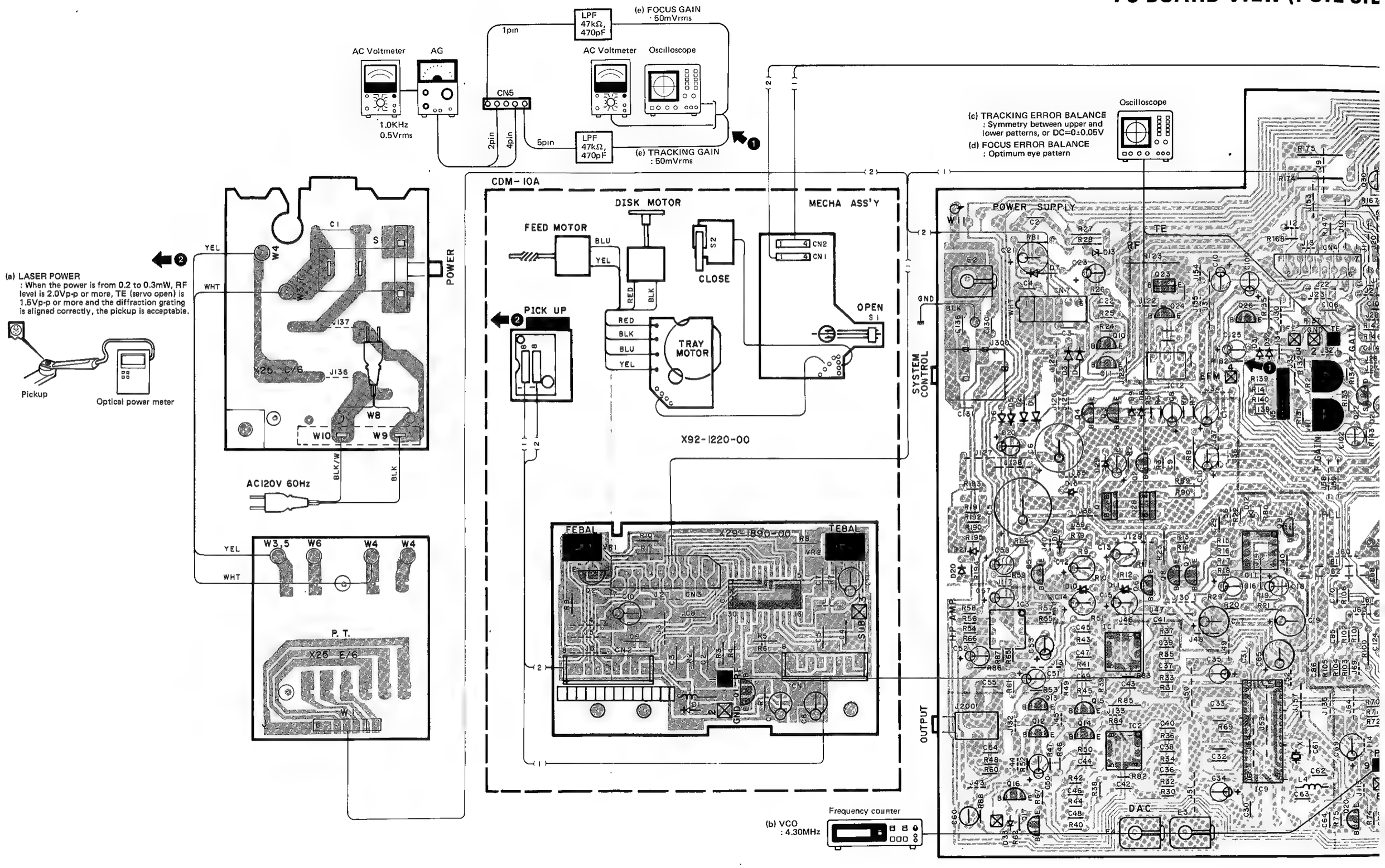
X29-1890-00

	B	C	E
Q1	4.8V	0.7V	5.1V
Q2	0.7V	0V	0V

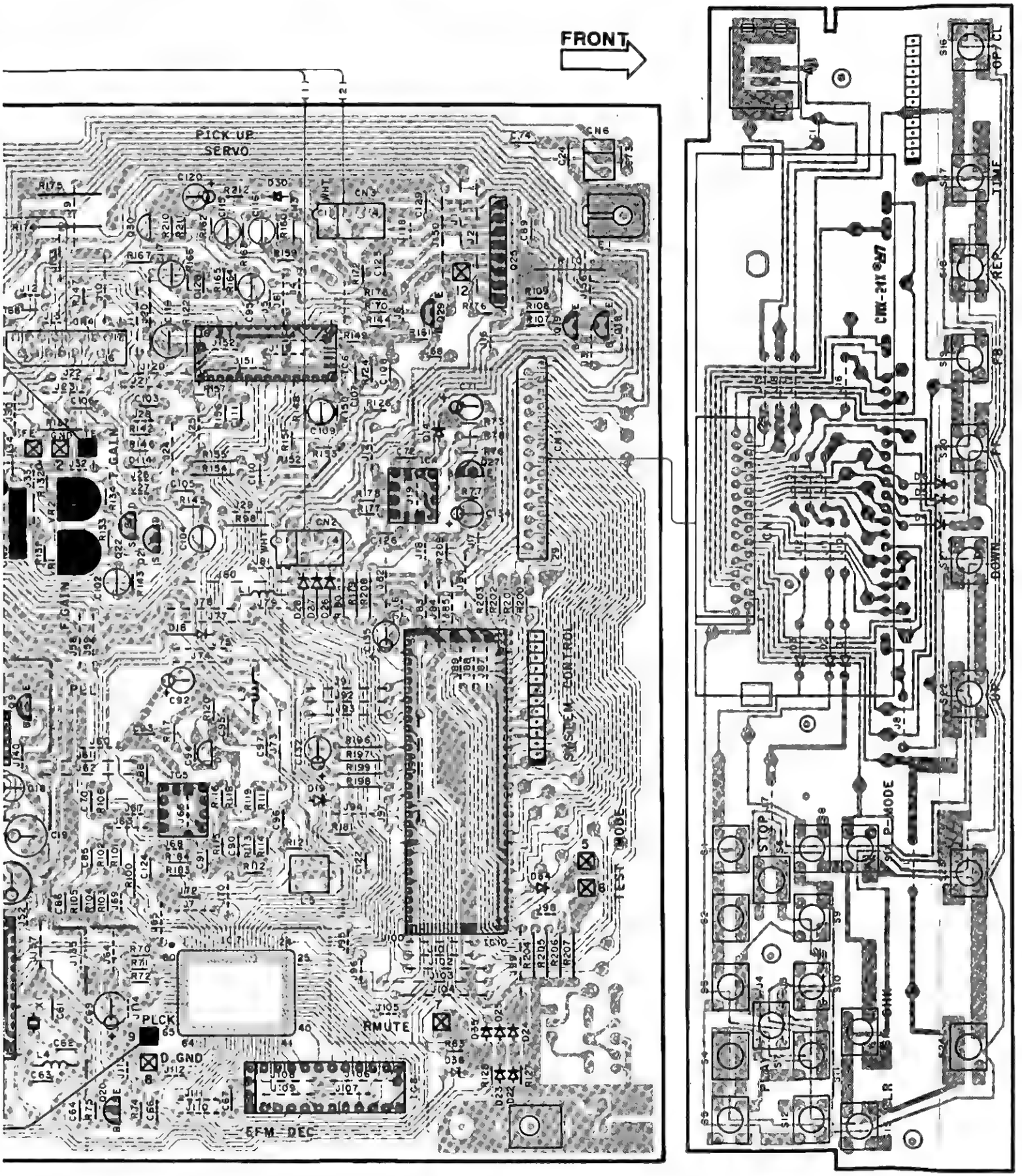
IC1

1 – 3	0V
5	4.8V
6	−5.0V
7 13	0V
15	−1.1V
16	1.3V
17	−5.0V
18	−0.2V
19, 20	0V
21	3.1V
22	0V
23	−3.5V
24, 25	0V
26	0.8V
27	4.3V
28	0.3V
29, 30	5.1V

PC BOARD VIEW (FOIL SID



V (FOIL SIDE VIEW)



Refer to the schematic diagram for the values of resistors and capacitors.

X25-331X-XX

	B	C	E
Q1	5.8V	8.4V	5.2V
Q2	0.6V	5.8V	0V
Q3, 4	−5.6V	−8.6V	−5.0V
Q5	6.7V	8.3V	6.1V
Q6	−6.8V	−8.6V	−6.1V
Q7, 8	7.7V	5.1V	–
Q9	−7.9V	−5.1V	−8.6V
Q10	−30.6V	−32.5V	-30.0V
Q11	−5.5V	−30.6V	−5.0V
Q12, 13	0.7V	0V	0V
Q14, 15	-6.1V	0V	0V
Q16	5.5V	−6.1V	6.1V
Q17	6.1V	3.4V	−6.1V
Q18	0.6V	8.4V	0V
Q19	0.6V	−8.6V	0V
Q20	0.6V	2.1V	0V
Q23	−0.7V	8.4V	0V
Q24	−0.7V	−8.6V	0V
Q26	4.5V	5.1V	5.1V
Q27	−7.3V	5.0V	0V
Q28	5.8V	8.4V	5.2V
Q29	0V	0.7V	0V
Q31	0V	4.2V	0V

	G	S	D
Q21, 22	0V	0V	0V

Q25

1	8.4V
2	0.6V
3	−0.6V
4	−1.1V
5	−8.6V
6 – 8	0V

IC1, 2

1 – 3	0V
4	−6.1V
5 – 7	0V
8	6.1V

IC4

1	−7.4V
2	5.1V
3	4.2V
4	−8.7V
5, 6	0V
7	0.6V
8	8.5V

IC5

1	0V
2, 3	2.6V
4	−8.7V
5, 6	0V
7	0.6V
8	8.5V

IC6

1 – 5	0V
6 – 10	5.1V
11 – 13	0V
14	−4.1V
15	5.1V
16	0.1V
17	−5.0V
18 – 20	0V
21	−0.7V
22	0V
23	−0.6V
24, 25	0V
26	5.1V
27	−0.6V
28 – 30	0V

IC7

1 – 3	0V
4	0.1V
5	4.3V
6	4.5V
8	0V
9	2.5V
10	0V
11	2.5V
12	0V
13 – 15	5.0V
16	4.9V
17	4.5V
18	0V
19	5.1V
20	0V
23, 24	0V
25	2.6V
26	0V
28	0V
29 – 32	0.6V
33	5.0V
34, 35	2.7V
36	2.2V
37	4.3V
38 – 44	2.4V
45	2.7V
46	2.3V
47	2.4V
48	2.8V
49	4.3V
50	2.0V
51	1.3V
52	0V
53	1.8V
55	0V
56	5.0V
57 – 59	0V

IC8

1 – 7	2.4V
8, 9	2.7V
10, 11	0.6V
12	0V
13, 14	0.6V
15	2.7V
16	2.2V
17	4.3V
18	2.0V
19	2.3V
20	2.0V
21	4.3V
22	2.8V
23	2.4V
24	5.0V

IC9

1, 2	5.1V
3	2.1V
4	5.1V
5	0V
7	2.6V
8	4.2V
9	0V
10	5.1V
11	3.0V
12	2.7V
13	5.1V
14, 15	−5.1V
16	−0.6V
17, 18	0V
19	−0.8V
20	0V
21	5.1V
22	0V
23	−3.7V
24 – 26	0V
27	−0.8V
28, 29	0V
30	−0.6V

IC10

1 – 4	−11.7V
5	0V
6	2.6V
7, 8	0V
9	5.0V
10 – 13	0V
14 – 16	5.1V
18	0.6V
19	5.1V
20	0.6V
21 – 24	0V
25 – 28	5.0V
30	1.3V
32	0V
35 – 38	0V
39	5.0V
40 – 48	−26.5V
54	−22.7V
55	−11.7V
56	−30.0V
57	−5.0V
58	−22.7V
59	−15.6V
61	−15.7V
62, 63	−22.0V
64	5.2V

IC11

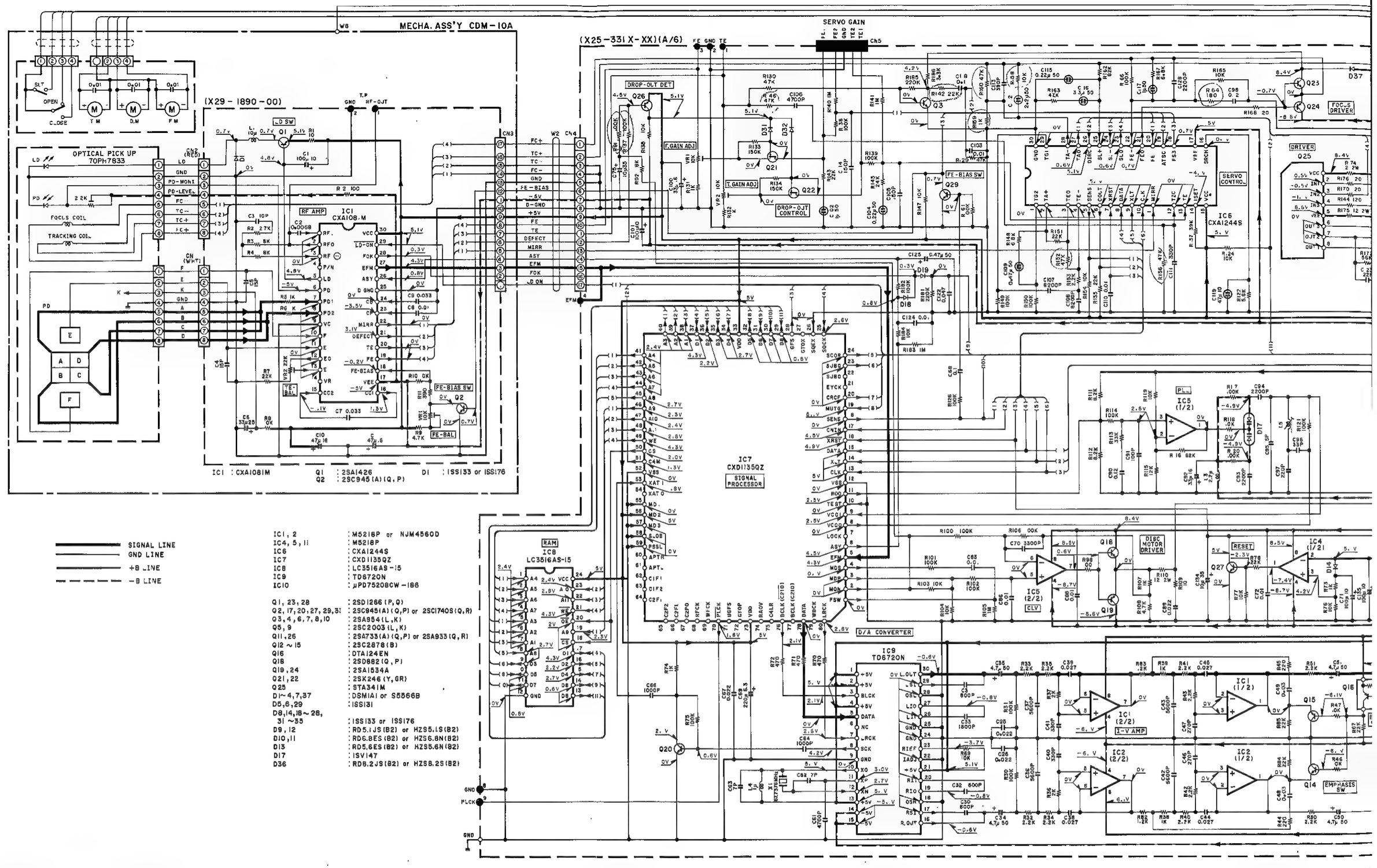
1	−2.8V
2, 3	0V
4	−8.6V
5, 6	3.0V
7	5.9V
8	8.4V

X29-1890-00

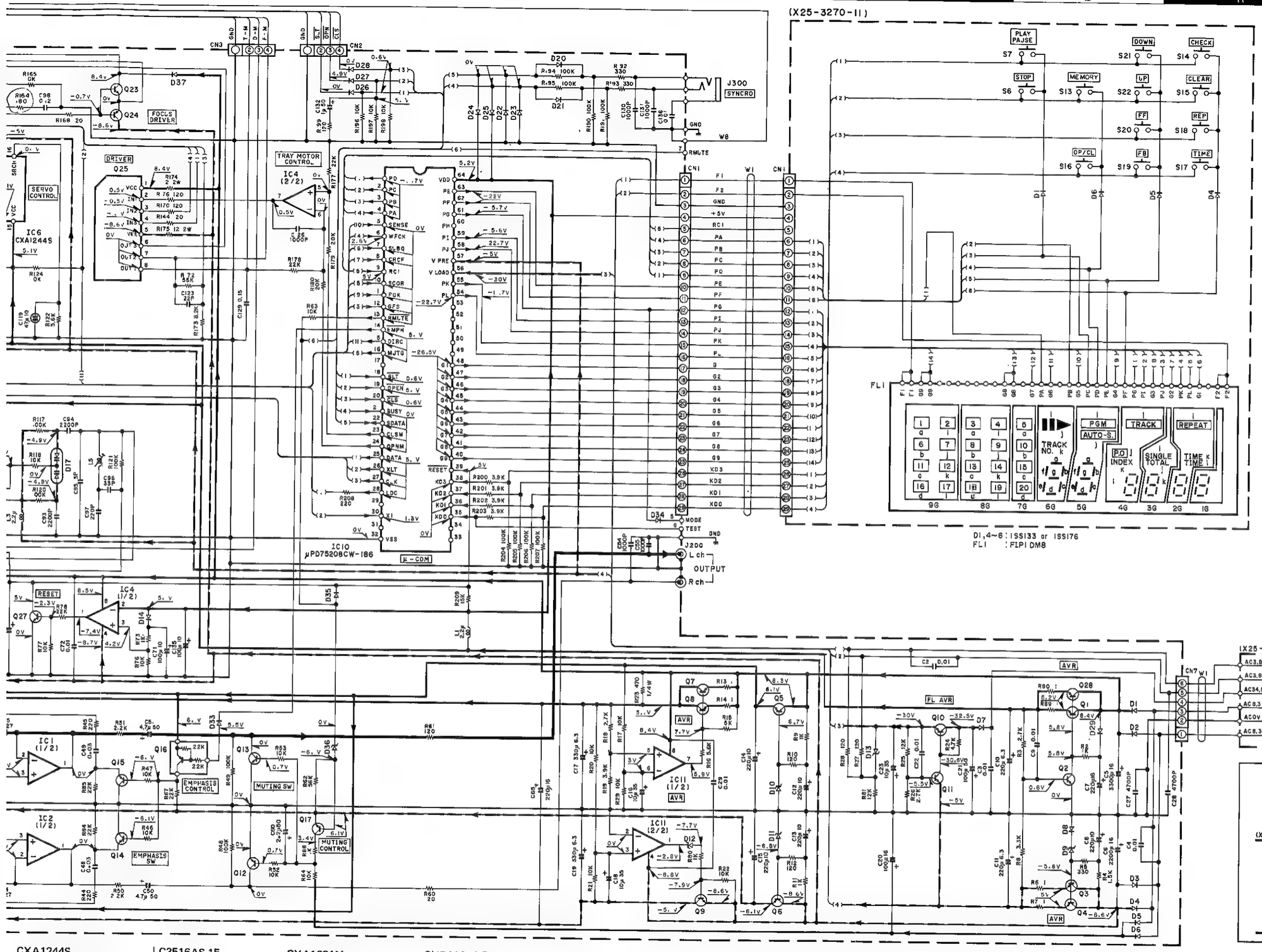
	B	C	E
Q1	4.8V	0.7V	5.1V
Q2	0.7V	0V	0V

IC1

1 – 3	0V
5	4.8V
6	−5.0V
7 – 13	0V
15	−1.1V
16	1.3V
17	−5.0V
18	−0.2V
19, 20	0V
21	3.1V
22	0V
23	−3.5V
24, 25	0V
26	0.8V
27	4.3V
28	0.3V
29, 30	5.1V


MECHA. ASS'Y CDM-10A
(X29-1890-00)
(X25-331X-XX)(A/6)
OPTICAL PICK UP
TOPH7833
SERVO GAIN
SERVO CONTRO.
DRIVER
FOCUS DRIVER
DISC MOTOR DRIVER
RESET
EMPHASIS SW
DROP-OUT DET
DROP-OUT CONTROL
F.GAIN ADJ
T.GAIN ADJ
FE-BIAS SW
FE-BAL
RF AMP
SIGNAL PROCESSOR
D/A CONVERTER
I-V AMP
CLV
RAM
IC1 : CXA1081M
Q1 : 2SA1426
Q2 : 2SC945(A)(Q,P)
D1 : ISS133 or ISS176
SIGNAL LINE
GND LINE
+B LINE
-B LINE
IC1, 2 : M5218P or NJM4560D
IC4, 5, 11 : M5218P
IC6 : CXA1244S
IC7 : CXD1135QZ
IC8 : LC3516AS-15
IC9 : TD6720N
IC10 : μPD75208CW-186
Q1, 23, 28 : 2SD1266(P,Q)
Q2, 17, 20, 27, 29, 31 : 2SC945(A)(Q,P) or 2SC1740S(Q,R)
Q3, 4, 6, 7, 8, 10 : 2SA954(L,K)
Q5, 9 : 2SC2003(L,K)
Q11, 26 : 2SA733(A)(Q,P) or 2SA933(Q,R)
Q12 ~ 15 : 2SC2878(B)
Q16 : DTA124EN
Q18 : 2SD882(Q,P)
Q19, 24 : 2SA1534A
Q21, 22 : 2SK246(Y,GR)
Q25 : STA341M
D1~4,7,37 : DSM1A1 or S5566B
D5,6,29 : ISS131
D8,14,18~28, 31~35 : ISS133 or ISS176
D9, 12 : RD5.1JS(B2) or HZS5.1S(B2)
D10, 11 : RD6.8ES(B2) or HZS6.8N(B2)
D13 : RD5.6ES(B2) or HZS5.6N(B2)
D17 : ISV147
D36 : RD8.2JS(B2) or HZS8.2S(B2)
DTA124EN
2SA1534A
2SA733(A)
2SA954
2SC2003
2SC2878
2SC945(A)
2SD882
2SD1266
2SA1426
2SA933S
2SC1740S
NJM4560D
M5218P
STA341M
2SK246
CXA1244S
TD6720N
LC351

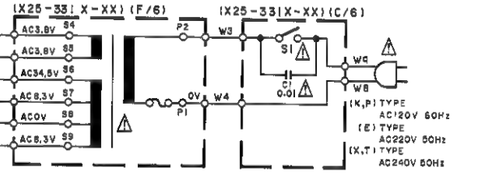
(X25-3270-11)

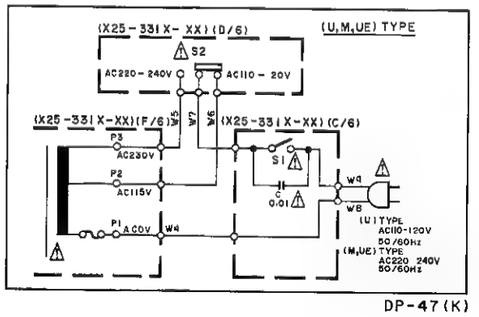


D1,4~6 : 1SS133 or 1SS176
FL1 : FIPI DM8

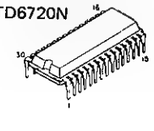
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

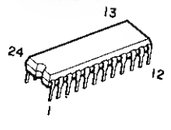




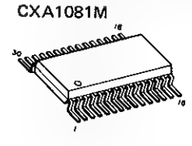
CXA1244S
TD6720N



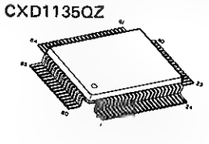
LC3516AS-15



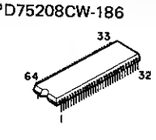
CXA1081M



CXD1135QZ



μPD75208CW-186

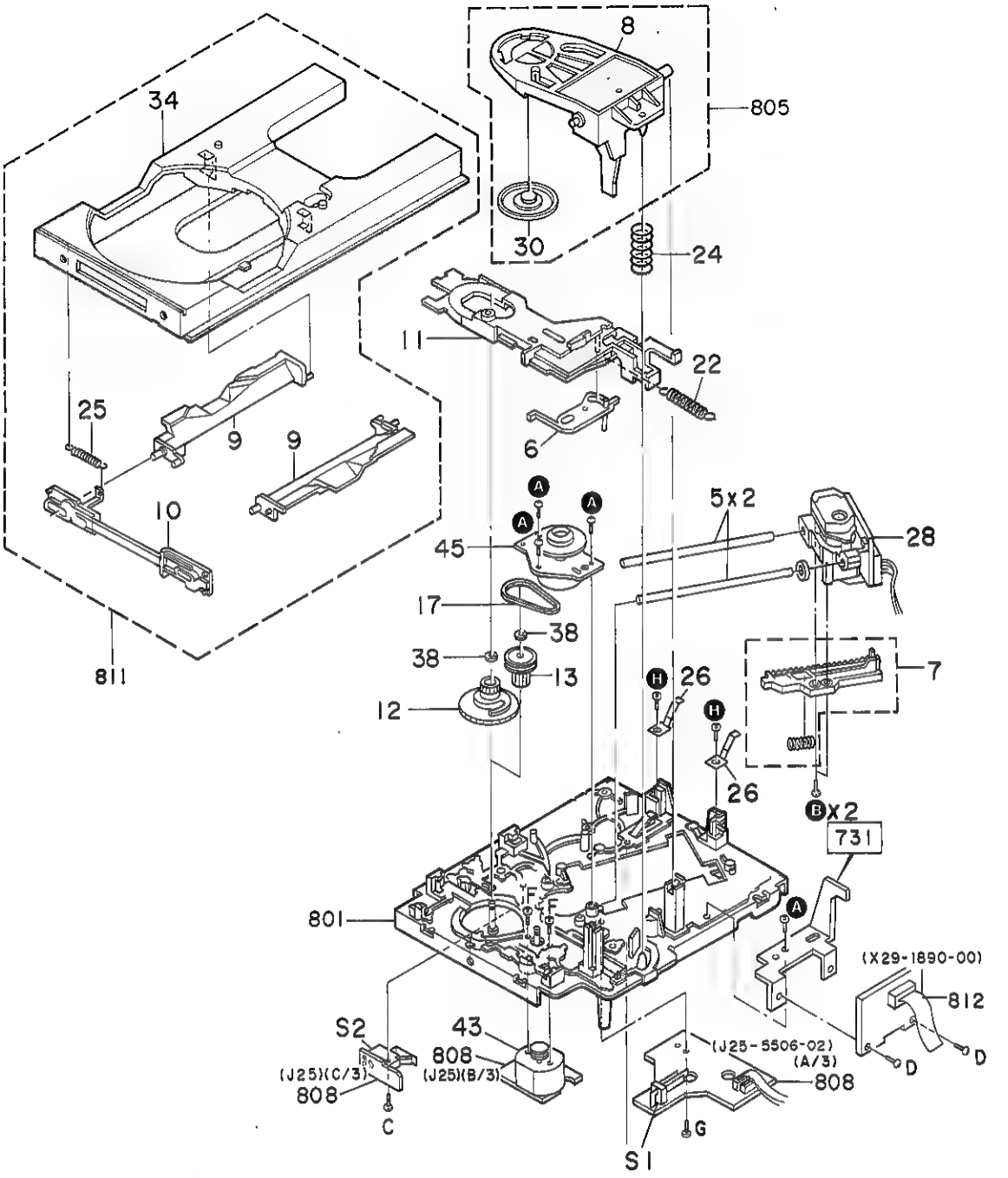


DP-47(K)

DP-47

KENWOOD

EXPLODED VIEW (MECHANISM)

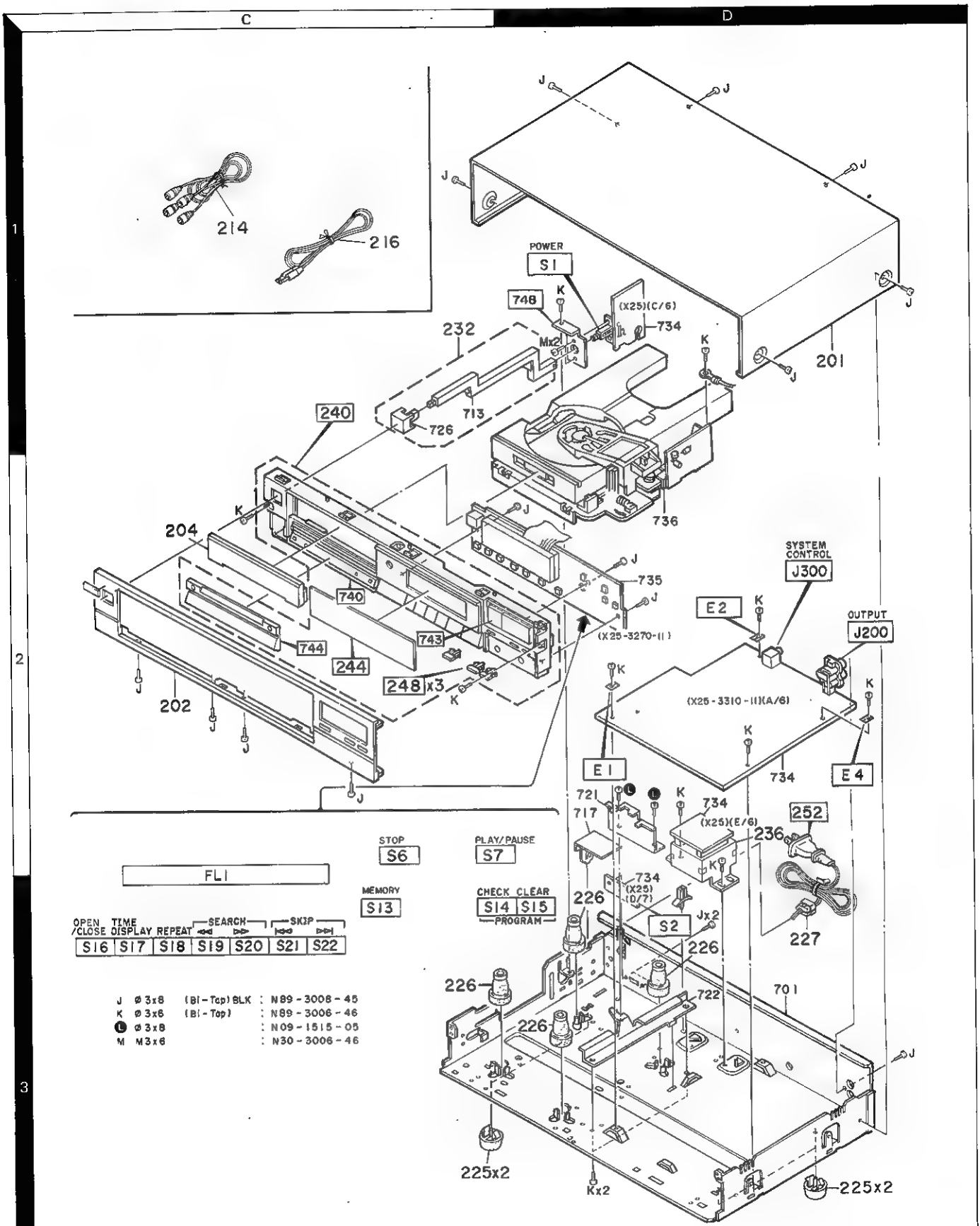


A	M2.6x8	: N09-1898-15
B		: N09-1899-05
C	M2x12 (Bi)	: N35-2012-46
D	ø2.6x6 (Br-Tap)	: N87-2606-46
F	M2x2.5	: N39-2025-46
G	ø2.6x8 (Br-Tap)	: N87-2608-46
H	M2x6	: N09-1532-05

DP-47

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

× New Parts
Parts without **Parts No.** are not supplied
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Telle ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			DP-47			
201	1D		A01-1542-01	METALLIC CABINET		
202	2C	*	A20-5501-02	PANEL		
204	2C		A29-0125-03	PANEL (TRAY)		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0094-03	WARRANTY CARD	UUE	
-			B46-0095-03	WARRANTY CARD	UUE	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0121-03	WARRANTY CARD	P	
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-		*	B50-8831-00	INSTRUCTION MANUAL(ENGLISH)		
-		*	B50-8832-00	INSTRUCTION MANUAL(FRENCH)	PMXE	
-		*	B50-8833-00	INSTRUCTION MANUAL(SPANISH)	M	
-		*	B50-8834-00	INSTRUCTION MANUAL(G,D,I)	E	
-		*	B50-8835-00	INSTRUCTION MANUAL(ARABIC)	M	
-			B58-0223-04	CAUTION CARD (PRE-SET 120V)	U	
-			B58-0513-04	CAUTION CARD (PRESET220-240)	UE	
-			B59-0092-00	SERVICE DIRECTORY	UUE	
214	1C		E30-0505-05	AUDIO CORD		
216	1C		E30-1392-05	CORD WITH PLUG		
-		*	H01-7808-04	ITEM CARTON CASE		
-		*	H10-3664-02	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-3665-02	POLYSTYRENE FOAMED FIXTURE		
-		*	H11-0016-04	POLYSTYRENE FOAMED BOARD		
-			H20-0417-14	PROTECTION COVER(460X370X360)	M	
-		*	H21-0255-04	PROTECTION SHEET		
-			H25-0223-04	PROTECTION BAG (750X350X0.03)	KPUUEX	
-			H25-0223-04	PROTECTION BAG (750X350X0.03)	TE	
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
225	3C,3D		J02-0366-15	FOOT		
226	3C,3D		J02-0369-05	INSULATOR		
⚠ 227	3D		J42-0083-05	POWER CORD BUSHING		
-			J61-0039-05	WIRE BAND		
232	1C		K29-3208-03	KNOB ASSY (POWER)		
⚠ 236	2D		L01-5161-05	POWER TRANSFORMER(120V)	KP	
⚠ 236	2D		L01-5162-05	POWER TRANSFORMER(230V)	XTE	
⚠ 236	2D		L01-5164-05	POWER TRANSFORMER(115/230V),	UMUE	
L	2D		N09-1515-05	TAPPING SCREW (3X8)		
			OPERATION UNIT (X25-3270-11)			
240	1C	*	A22-0970-03	SUB PANEL ASSY		
244	2C	*	B03-2430-03	DRESSING PLATE (DISPLAY)		
CN1			E10-2904-05	FLAT CABLE CONNECTOR		
248	2C		K29-2654-04	KNOB (BUTTON) P-M0,PROGRAM		
S6 -7	2C		S40-1064-05	PUSH SWITCH (STOP,PLAY/PAUSE)		
S13 -22	3C		S40-1064-05	PUSH SWITCH (P-M0,SEARCH)		
D1 -6			1SS133	DIODE		
D1 -6			1SS176	DIODE		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格		Destination 仕向	Remarks 備考
FL1	1C		FJP11DM8	FLURESCENT INDICATOR TUBE			
ELECTRIC UNIT (X25-331X-XX) 0-11 : K,P 0-22 : U,M,UE 0-71 : X 0-51 : T 2-71 : E							
⚠ C1			C91-0647-05	CERAMIC	0.01UF	P	
C2 -4			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C5			CE04KW1C332M	ELECTRO	3300UF	16WV	
C6			CE04KW1C222M	ELECTRO	2200UF	16WV	
C7			CE04KW1C221M	ELECTRO	220UF	16WV	
C8			CE04KW1A221M	ELECTRO	220UF	10WV	
C9			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C10 ,11			CE04KW0J221M	ELECTRO	220UF	6.3WV	
C12 -15			CE04KW1A221M	ELECTRO	220UF	10WV	
C16			CE04KW1V100M	ELECTRO	10UF	35WV	
C17			CE04KW0J331M	ELECTRO	330UF	6.3WV	
C18			CE04KW1V100M	ELECTRO	10UF	35WV	
C19			CE04KW0J331M	ELECTRO	330UF	6.3WV	
C20			CE04KW1C101M	ELECTRO	100UF	16WV	
C21			CE04KW1H101M	ELECTRO	100UF	50WV	
C22			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C23			CE04KW1V100M	ELECTRO	10UF	35WV	
C25 ,26			CK45FF1H223Z	CERAMIC	0.022UF	Z	
C29			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C30 -33			CQ09FS1H182J	POLYSTY	1800PF	J	
C34 ,35			CE04KW1H4R7M	ELECTRO	4.7UF	50WV	
C36 ,37			CF92FV1H562J	MF	5600PF	J	
C38 ,39			CF92FV1H273J	MF	0.027UF	J	
C40 ,41			CC45FSL1H331J	CERAMIC	330PF	J	
C42 ,43			CF92FV1H562J	MF	5600PF	J	
C44 ,45			CF92FV1H273J	MF	0.027UF	J	
C46 ,47			CC45FSL1H271J	CERAMIC	270PF	J	
C48 ,49			CF92FV1H303J	MF	0.030UF	J	
C50 ,51			CE04KW1H4R7M	ELECTRO	4.7UF	50WV	
C54 ,55			CK45FB1H102K	CERAMIC	1000PF	K	
C60			C90-1350-05	NP-ELEC	2.2UF	50WV	
C61			CK45FF1H472Z	CERAMIC	4700PF	Z	
C62 ,63			CC45FSL1H070D	CERAMIC	7.0PF	D	
C64			CK45FB1H102K	CERAMIC	1000PF	K	
C65			CE04KW1C221M	ELECTRO	220UF	16WV	
C66			CK45FB1H102K	CERAMIC	1000PF	K	
C67			CK45FF1H223Z	CERAMIC	0.022UF	Z	
C68			CF92FV1H104J	MF	0.10UF	J	
C69			CE04KW0J221M	ELECTRO	220UF	6.3WV	
C70			CK45FB1H332K	CERAMIC	3300PF	K	
C71			CE04KW1A101M	ELECTRO	100UF	10WV	
C72			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C75			CF04KW1V100M	ELECTRO	10UF	35WV	
C85 ,86			CF92FV1H103J	MF	0.010UF	J	
C88			CK45FF1H103Z	CERAMIC	0.010UF	Z	
C89			CK45FF1H223Z	CERAMIC	0.022UF	Z	
C90			CF92FV1H124J	MF	0.12UF	J	
C91			CC45FSL1H101J	CERAMIC	100PF	J	
C92			CE04KW1C330M	ELECTRO	33UF	16WV	
C93 ,94			CK45FB1H222K	CERAMIC	2200PF	K	
C95			CC45FUJ1H050C	CERAMIC	5.0PF	C	
C96			CC45FUJ1H330J	CERAMIC	33PF	J	

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
C97			CC45FUJ1H221J	CERAMIC 220PF J		
C98			CF92FV1H124J	MF 0.12UF J		
C100			CE04KW1A101M	ELECTRO 100UF 10WV		
C101			CE04KW1C330M	ELECTRO 33UF 16WV		
C102			C90-1349-05	NP-ELEC 1UF 50WV		
C103			CF92FV1H103J	MF 0.010UF J		
C104			C90-1456-05	NP-ELEC 0.22UF 50WV		
C105			CC45FSL1H151J	CERAMIC 150PF J		
C106			CK45FF1H472Z	CERAMIC 4700PF Z		
C107,108			CF92FV1H822J	MF 8200PF J		
C109			C90-1331-05	NP-ELEC 0.47UF 50WV		
C110			CK45FF1H103Z	CERAMIC 0.010UF Z		
C111			CC45FSL1H331J	CERAMIC 330PF J		
C112			C90-1350-05	NP-ELEC 2.2UF 50WV		
C113			CK45FB1H391K	CERAMIC 390PF K		
C114			CC45FSL1H151J	CERAMIC 150PF J		
C115			C90-1456-05	NP-ELEC 0.22UF 50WV		
C116			C90-1351-05	NP-ELEC 3.3UF 50WV		
C117			C90-1349-05	NP-ELEC 1UF 50WV		
C118			CF92FV1H104J	MF 0.10UF J		
C119			C90-1334-05	NP-ELEC 47UF 10WV		
C122			CF92FV1H473J	MF 0.047UF J		
C123			CC45FSL1H220J	CERAMIC 22PF J		
C124			CF92FV1H103J	MF 0.010UF J		
C125			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C126			CK45FB1H102K	CERAMIC 1000PF K		
C128			CK45FB1H222K	CERAMIC 2200PF K		
C129			CF92FV1H154J	MF 0.15UF J		
C130,131			CK45FB1H102K	CERAMIC 1000PF K		
C132			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C134			CE04KW1V100M	ELECTRO 10UF 35WV		
C135			CE04KW1A101M	ELECTRO 100UF 10WV		
C136			CK45FF1H103Z	CERAMIC 0.010UF Z		
⚠ 252	2D	*	E30-2423-05	AC POWER CORD	KP	
⚠ 252	2D		E30-0459-05	AC POWER CORD	E	
⚠ 252	2D		E30-1341-05	AC POWER CORD	X	
⚠ 252	2D		E30-1416-05	AC POWER CORD	T	
⚠ 252	2D		E30-2284-05	AC POWER CORD	UMUE	
CN1			E10-2903-05	FLAT CABLE CONNECTOR		
CN4			E10-1705-05	FLAT CABLE CONNECTOR		
J200	2D		E13-0235-05	PHONO JACK(2P) OUTPUT		
J300	2D		E11-0164-05	MINIATURE PHONE JACK(3P)SYNCRO		
-			J61-0307-05	WIRE BAND		
L1			L40-2292-17	SMALL FIXED INDUCTOR(2.2UH,M)		
L3			L40-2292-17	SMALL FIXED INDUCTOR(2.2UH,M)		
L4			L40-1092-17	SMALL FIXED INDUCTOR(1UH,M)		
L5			L32-0328-15	OSCILATING COIL		
X1			L77-1128-05	CRYSTAL RESONATOR		
R110			RS14KB3D120J	FL-PROOF RS 12 J 2W		
R174,175			RS14KB3D120J	FL-PROOF RS 12 J 2W		
VR1,2			R12-3126-05	TRIMMING POT.(10K)T/F GAIN		
⚠ S1	1D		S40-1103-05	PUSH SWITCH (POWER TYPE)		
⚠ S2	3D		S31-2128-05	SLIDE SWITCH (POWER TYPE)	UMUE	

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Telle ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
D1 -4			DSM1A1	DIODE		
D5 ,6			1SS131	DIODE		
D7			DSM1A1	DIODE		
D8			1SS133	DIODE		
D8			1SS176	DIODE		
D9			HZS5.1S(B2)	ZENER DIODE		
D9			RD5.1JS(B2)	ZENER DIODE		
D10 ,11			HZS6.8N(B2)	ZENER DIODE		
D10 ,11			RD6.8ES(B2)	ZENER DIODE		
D12			HZS5.1S(B2)	ZENER DIODE		
D12			RD5.1JS(B2)	ZENER DIODE		
D13			HZS5.6N(B2)	ZENER DIODE		
D13			RD5.6ES(B2)	ZENER DIODE		
D14			1SS133	DIODE		
D14			1SS176	DIODE		
D17			1SV147	VARISTOR		
D18 -28			1SS133	DIODE		
D18 -28			1SS176	DIODE		
D29			1SS131	DIODE		
D31 -35			1SS133	DIODE		
D31 -35			1SS176	DIODE		
D36			HZS8.2S(B2)	ZENER DIODE		
D36			RD8.2JS(B2)	ZENER DIODE		
D37			DSM1A1	DIODE		
D37			S5566B	DIODE		
IC1 ,2			M5218P	IC(OP AMP X2)		
IC4 ,5			M5218P	IC(OP AMP X2)		
IC6			CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC7			CXD1135QZ	IC(DIGITAL SIGNAL PROCESSOR)		
IC8			LC3516AS-15	IC(2KX8 RAM)		
IC9			TD6720N	IC(16BIT HI-FI D/A CONVERTER)		
IC10		*	UPD75208CW-186	IC(MICROPROCESSOR)		
IC11			M5218P	IC(OP AMP X2)		
IC11			NJM4560D	IC(OP AMP X2)		
Q1			2SD1266(Q,P)	TRANSISTOR		
Q2			2SC1740S(Q,R)	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
Q3 ,4			2SA954(L,K)	TRANSISTOR		
Q5			2SC2003(L,K)	TRANSISTOR		
Q6 -8			2SA954(L,K)	TRANSISTOR		
Q9			2SC2003(L,K)	TRANSISTOR		
Q10			2SA954(L,K)	TRANSISTOR		
Q11			2SA733(A)(Q,P)	TRANSISTOR		
Q11			2SA933S(Q,R)	TRANSISTOR		
Q12 -15			2SC2878(B)	TRANSISTOR		
Q16			DTA124EN	DIGITAL TRANSISTOR		
Q17			2SC1740S(Q,R)	TRANSISTOR		
Q17			2SC945(A)(Q,P)	TRANSISTOR		
Q18			2SD882(Q,P)	TRANSISTOR		
Q19			2SA1534A	TRANSISTOR		
Q20			2SC1740S(Q,R)	TRANSISTOR		
Q20			2SC945(A)(Q,P)	TRANSISTOR		
Q21 ,22			2SK246(Y,GR)	FET		
Q23			2SD1266(Q,P)	TRANSISTOR		
Q24			2SA1534A	TRANSISTOR		

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
Q25			STA341M	TRANSISTOR		
Q26			2SA733(A)(Q,P)	TRANSISTOR		
Q26			2SA933S(Q,R)	TRANSISTOR		
Q27			2SC1740S(Q,R)	TRANSISTOR		
Q27			2SC945(A)(Q,P)	TRANSISTOR		
Q28			2SD1266(Q,P)	TRANSISTOR		
Q29			2SC1740S(Q,R)	TRANSISTOR		
Q29			2SC945(A)(Q,P)	TRANSISTOR		
Q31			2SC1740S(Q,R)	TRANSISTOR		
Q31			2SC945(A)(Q,P)	TRANSISTOR		
CONTROL CIRCUIT UNIT (X29-1890-00)						
C1			CE04JW1A101M	ELECTRO 100UF 10WV		
C2			CF92FV1H682J	MF 6800PF J		
C3			CC45FSL1H100D	CERAMIC 10PF D		
C4			CC45FSL1H150J	CERAMIC 15PF J		
C5			CC45FSL1H150J	CERAMIC 15PF J		
C6			CE04JW1E330M	ELECTRO 33UF 25WV		
C7			CF92FV1H333J	MF 0.033UF J		
C8			CF92FV1H103J	MF 0.010UF J		
C9			CF92FV1H333J	MF 0.033UF J		
C10 ,11			CE04KW1C470M	ELECTRO 47UF 16WV		
CN3			E10-1705-05	FLAT CABLE CONNECTOR		
L1			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
VR1			R12-3100-05	TRIMMING POT.(10K) FE BAL		
VR2			R12-3101-05	TRIMMING POT.(22K) TE BAL		
D1			1SS133	DIODE		
IC1			CXA1081M	IC(RF AMP)		
Q1			2SA1426	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
MECHANISM ASS'Y (X92-1220-00)						
C1 ,2			C91-0769-05	CERAMIC 0.01UF M		
4	3B		D13-0649-08	GEAR		
5	2B		D10-2011-04	ROD (PU)		
6	1B		D10-1738-04	ARM (SW)		
7	2B		D13-0650-05	GEAR ASSY		
8	1B		D10-1741-13	ARM (CLAMPER)		
9	1A		D10-1742-02	ARM (LIFTER)		
10	2A		D10-1743-13	SLIDER (LIFTER)		
11	1A		D10-1782-24	SLIDER ASSY		
12	2A		D13-0359-13	GEAR (MAIN)		
13	2B		D13-0360-04	GEAR		
17	2A		D16-0140-14	BELT		
18	3B	*	D40-0586-05	DRIVE MECHANISM ASSY		
22	1B		G01-1890-04	EXTENSION SPRING (SLIDER)		
24	1B		G01-1892-14	COMPRESSION SPRING(ARM)		
25	1A		G01-1893-04	EXTENSION SPRING (TRAY ASSY)		
26	2B	*	G02-0479-04	FLAT SPRING		
28	2B	*	J91-0347-05	PICKUP		
30	1B		J11-0086-04	CLAMPER		
34	1A		J99-0038-01	TRAY		
38	2A,2B		N19-0366-04	FLAT WASHER (GEAR)		

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
A	2B	*	N09-1898-15	MACHINE SCREW		
B	2B		N09-1899-05	MACHINE SCREW		
S1	3B		S46-1087-05	LEAF SWITCH (OPEN/CLS)		
S2	3A		S33-1019-05	LEVER SWITCH (SLT)		
43	3A		T42-0097-25	DC MOTOR (LOADING)		
44	3A	*	T42-0449-08	MOTOR ASSY		
45	2A	*	T42-0447-04	MOTOR ASSY (SPINDLE)		

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DP-47

SPECIFICATIONS

Number of channels	2 channels
Frequency response	20Hz – 20 kHz, ± 1 dB
Dynamic range	More than 92 dB at 1 kHz
Signal to noise ratio	More than 94 dB
Total harmonic distortion	Less than 0.007% at 1 kHz
Channel separation	More than 88 dB at 1 kHz
Wow & flutter	Unmeasurable limit
Line output level/impedance	1.6 V/3.3 kohms
Playing speed	1.2 – 1.4 m/sec (constant linear velocity)
Quantization	16 bits linear 1 channel
Sampling frequency	44.1 kHz
Power consumption	15 W
Dimensions	W 420 mm (16-9/16") H 90 mm (3-9/16") D 262 mm (10-5/16")
Weight (Net)	3.8 kg (8.4 lb)

Note:
We follow a policy of advancements in development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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650 Clark Drive, Mount Olive, NJ 07828, U.S.A.

KENWOOD ELECTRONICS CANADA INC.
P.O. Box 1075 959 Gana Court, Mississauga, Ontario, Canada L4T 4C2

KENWOOD ELECTRONICS BENELUX N.V.
Mechelsesteenweg 418 B-1930 Zaventem, Belgium

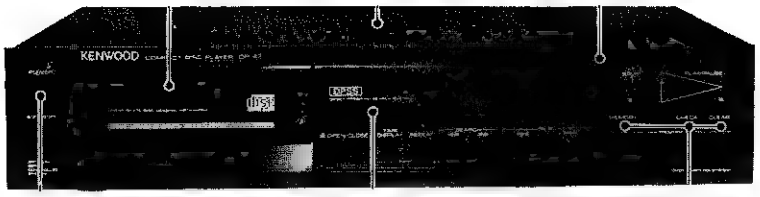
KENWOOD ELECTRONICS DEUTSCHLAND GMBH
Rembrucker-Str. 15, 6056 Heusenstamm West Germany

TRIO-KENWOOD FRANCE S.A.
Hi-Fi·VIDEO·CAR Hi-Fi
13, Boulevard Ney, 75018 Paris, France

TRIO-KENWOOD U.K. LTD.
17 Bristol Road, The Metropolitan Centre, Greenford, Middx UB6 8UP England

KENWOOD ELECTRONICS AUSTRALIA PTY. LTD.
4E Woodcock Place, Lane Cove, N.S.W. 2066, Australia

KENWOOD & LEE ELECTRONICS, LTD.
Wang Kee Building, 4th Floor, 34-37, Connaught Road, Central, Hong Kong



SPECIFICATIONS

Number of channels	2 channels
Frequency response	20Hz – 20 kHz, ± 1 dB
Dynamic range	More than 92 dB at 1 kHz
Signal to noise ratio	More than 94 dB
Total harmonic distortion	Less than 0.007% at 1 kHz
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Power consumption	15 W
Dimensions	W 420 mm (16-9/16")
	H 90 mm (3-9/16")
	D 262 mm (10-5/16")
Weight (Net)	3.8 kg (8.4 lb)

DP-47

KENWOOD

TROUBLESHOOTING

From August 1988, two types of signal processors will be provided. For repair, use the same IC as used in a product to be repaired.

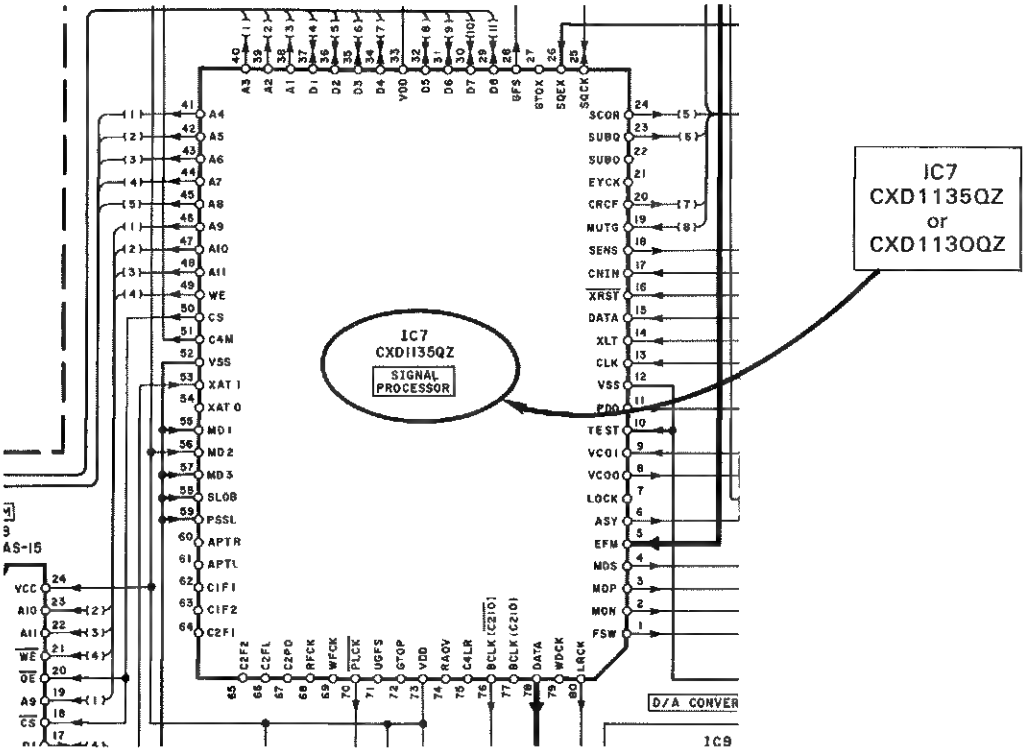
Original signal processor: CXD1135QZ

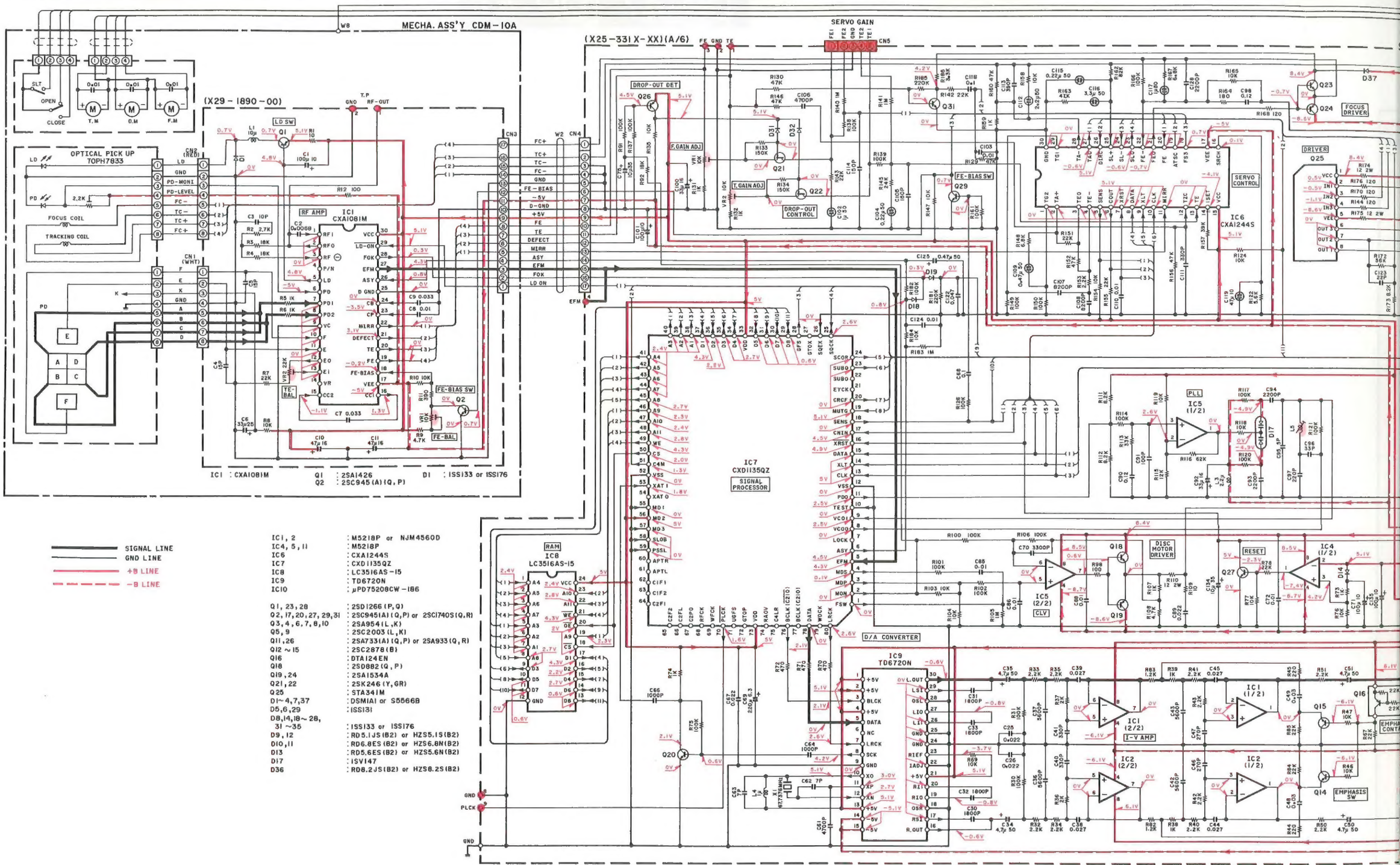
New type signal processor: CXD1130QZ

Difference between the CXD1135QZ and CXD1130QZ consists in presence or absence of the digital filter as well as characteristics of the digital filter.

Though output voltage of the new type signal processor is lower than the old type (by approx. 4 dB), it is considered that there are no problems in practical use.

Output voltage will be omitted from specifications in the instruction manual.



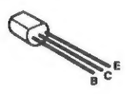


SIGNAL LINE
GND LINE
+B LINE
-B LINE

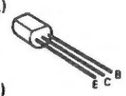
IC1, 2	: M5218P or NJM4560D
IC4, 5, 11	: M5218P
IC6	: CXA1244S
IC7	: CXD1135QZ
IC8	: LC3516AS-15
IC9	: TD6720N
IC10	: μPD75208CW-186
Q1, 23, 28	: 2SD1266 (P, Q)
Q2, 17, 20, 27, 29, 31	: 2SC945(A) (Q, P) or 2SC1740S (Q, R)
Q3, 4, 6, 7, 8, 10	: 2SA954 (L, K)
Q5, 9	: 2SC2003 (L, K)
Q11, 26	: 2SA733(A) (Q, P) or 2SA933 (Q, R)
Q12 ~ 15	: 2SC2878 (B)
Q16	: DTA124EN
Q18	: 2SD882 (Q, P)
Q19, 24	: 2SA1534A
Q21, 22	: 2SK246 (Y, GR)
Q25	: STA341M
D1~4, 7, 37	: DSM1A1 or S5566B
D5, 6, 29	: ISS131
D8, 14, 18~28, 31~35	: ISS133 or ISS176
D9, 12	: RD5.1JS(B2) or HZS5.1S(B2)
D10, 11	: RD6.8ES(B2) or HZS6.8N(B2)
D13	: RD5.6ES(B2) or HZS5.6N(B2)
D17	: ISV147
D36	: RD8.2JS(B2) or HZS8.2S(B2)

IC1 : CXA1081M Q1 : 2SA1426 Q2 : 2SC945(A)(Q, P) D1 : ISS133 or ISS176

DTA124EN

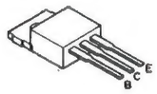


2SA1534A
2SA733(A)
2SA954
2SC2003
2SC2878
2SC945(A)



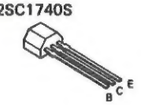
2SD882

2SD1266



2SA1426

2SA933S
2SC1740S



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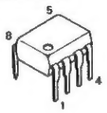
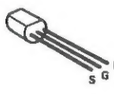


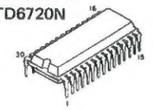
M5218P

STA341M

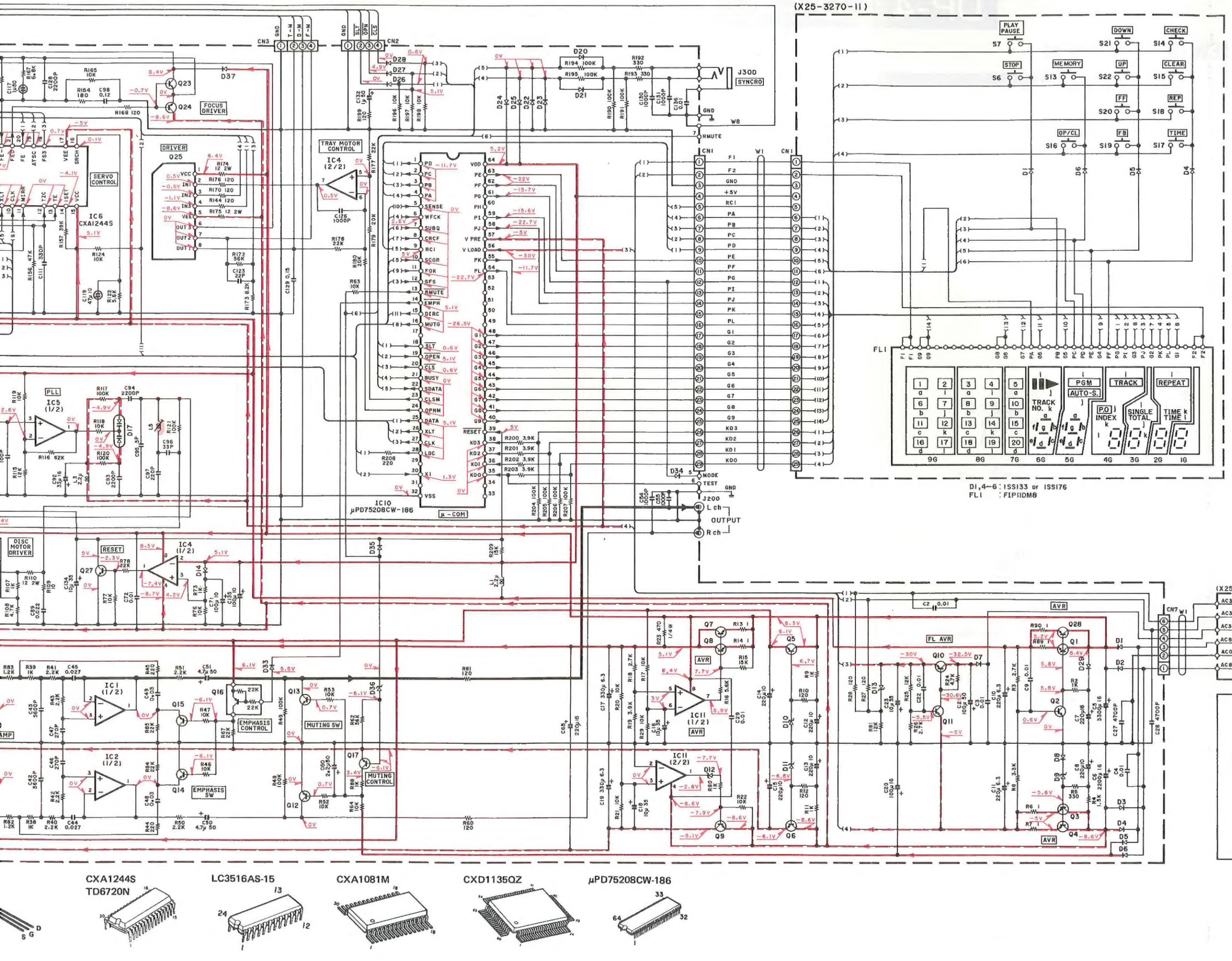
2SK246



CXA1244S
TD6720N



LC3516AS



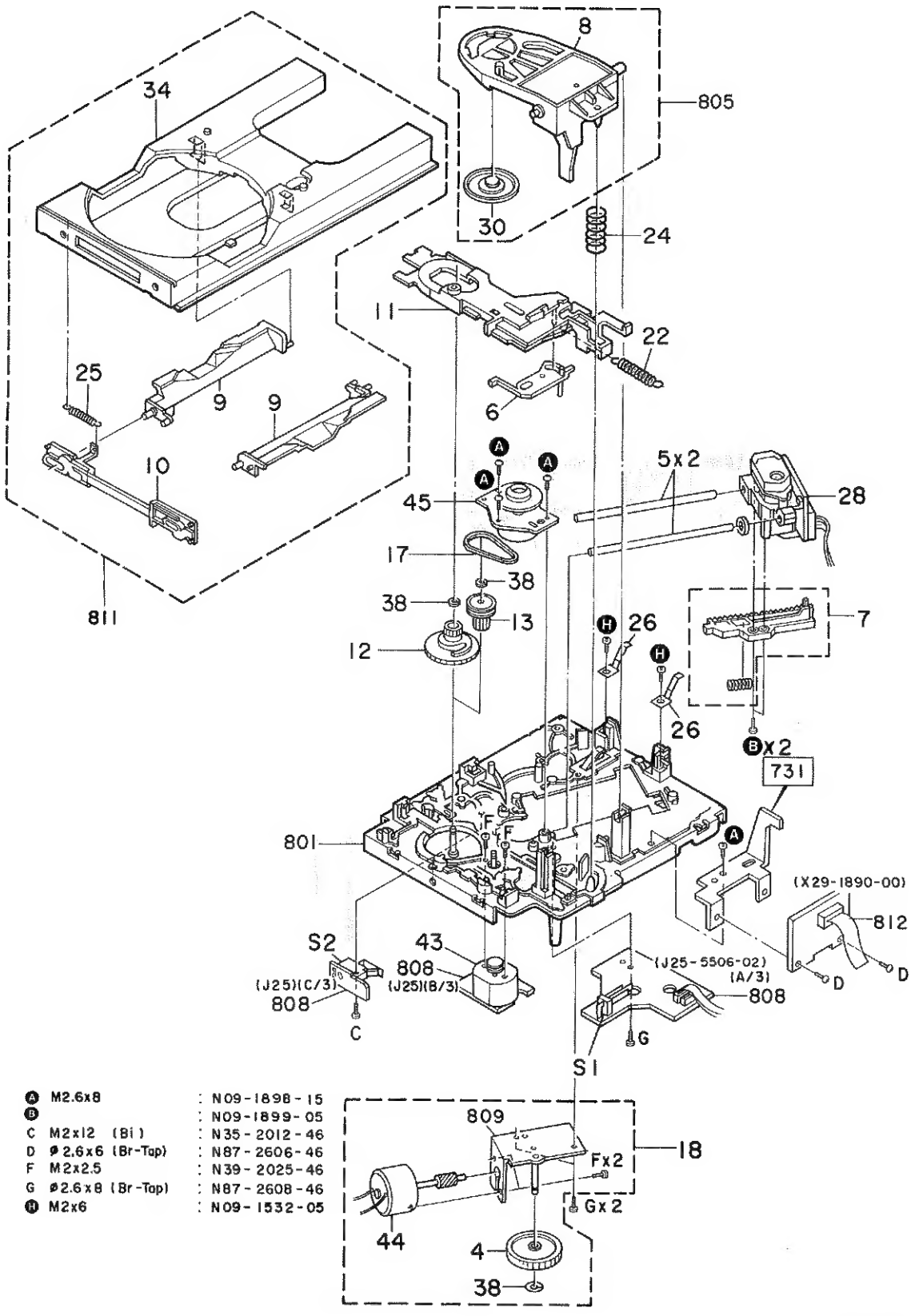
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen. Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

DP-47 (K)

DP-47

EXPLODED VIEW (MECHANISM)



DP-47

Parts with the exploded numbers larger than 700 are not supplied.

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
MECHANISM ASS'Y (X92-1220-00)						
C1 ,2			C91-0769-05	CERAMIC 0.01UF M		
4	3B		D13-0649-08	GEAR		
5	2B		D10-2011-04	ROD (PU)		
6	1B		D10-1738-04	ARM (SW)		
7	2B		D13-0650-05	GEAR ASSY		
8	1B		D10-1741-13	ARM (CLAMPER)		
9	1A		D10-1742-02	ARM (LIFTER)		
10	2A		D10-1743-13	SLIDER (LIFTER)		
11	1A		D10-1782-24	SLIDER ASSY		
12	2A		D13-0359-13	GEAR (MAIN)		
13	2B		D13-0360-04	GEAR		
17	2A		D16-0140-14	BELT		
18	3B	*	D40-0586-05	DRIVE MECHANISM ASSY		
22	1B		G01-1890-04	EXTENSION SPRING (SLIDER)		
24	1B		G01-1892-14	COMPRESSION SPRING(ARM)		
25	1A		G01-1893-04	EXTENSION SPRING (TRAY ASSY)		
26	2B	*	G02-0479-04	FLAT SPRING		
28	2B	*	J91-0347-05	PICKUP		
30	1B		J11-0086-04	CLAMPER		
34	1A		J99-0038-01	TRAY		
38	2A,2B		N19-0366-04	FLAT WASHER (GEAR)		
A	2B	*	N09-1898-15	MACHINE SCREW		
B	2B		N09-1899-05	MACHINE SCREW		
S1	3B		S46-1087-05	LEAF SWITCH (NPN/CLS)		
S2	3A		S33-1019-05	LEVER SWITCH (SLT)		
43	3A		T42-0097-25	DC MOTOR (LOADING)		
44	3A	*	T42-0449-08	MOTOR ASSY		
45	2A	*	T42-0447-04	MOTOR ASSY (SPINDLE)		

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